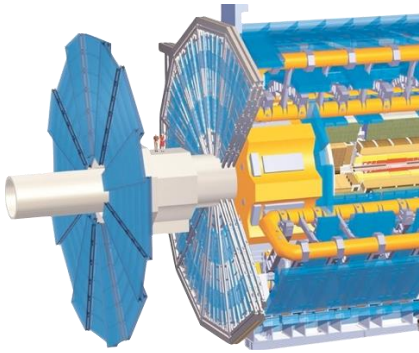
TEXAS
The University of Texas at Austin

ATLAS EXPERIMENT



UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

Chen-Kai Hsu

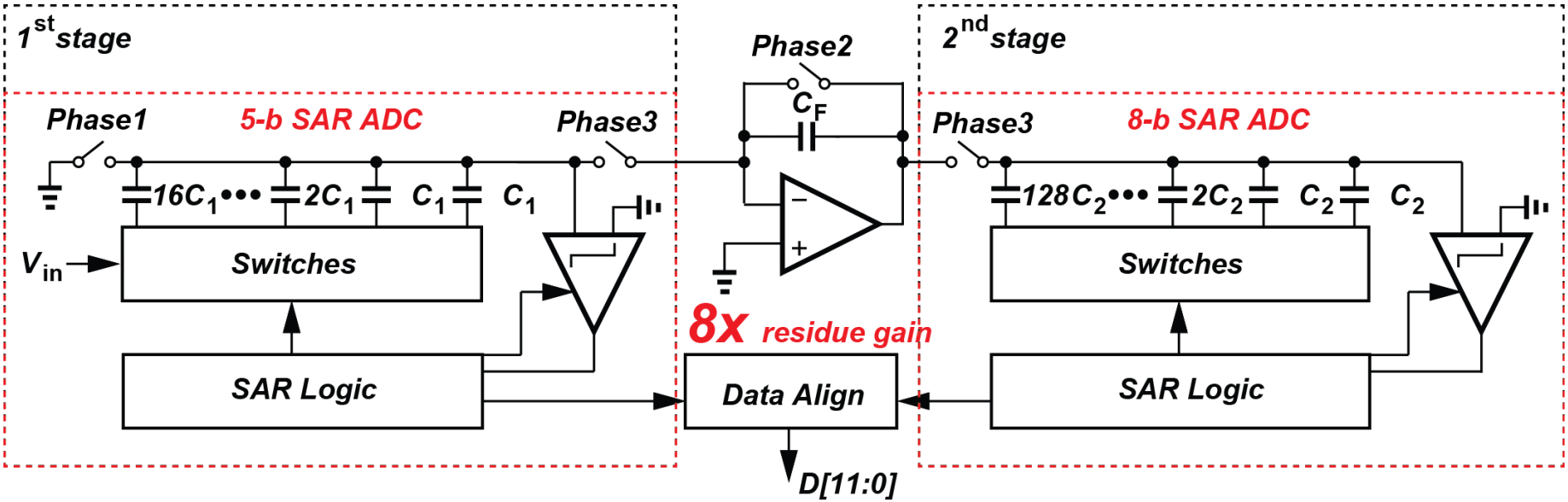
ckhsu@utexas.edu

Dec 2, 2016

Outline

- Linearity Issue
- SAR Logic redesign
- OPAMP corner simulation

Linearity Issue



- Amplifier Linearity Test

  Resut:

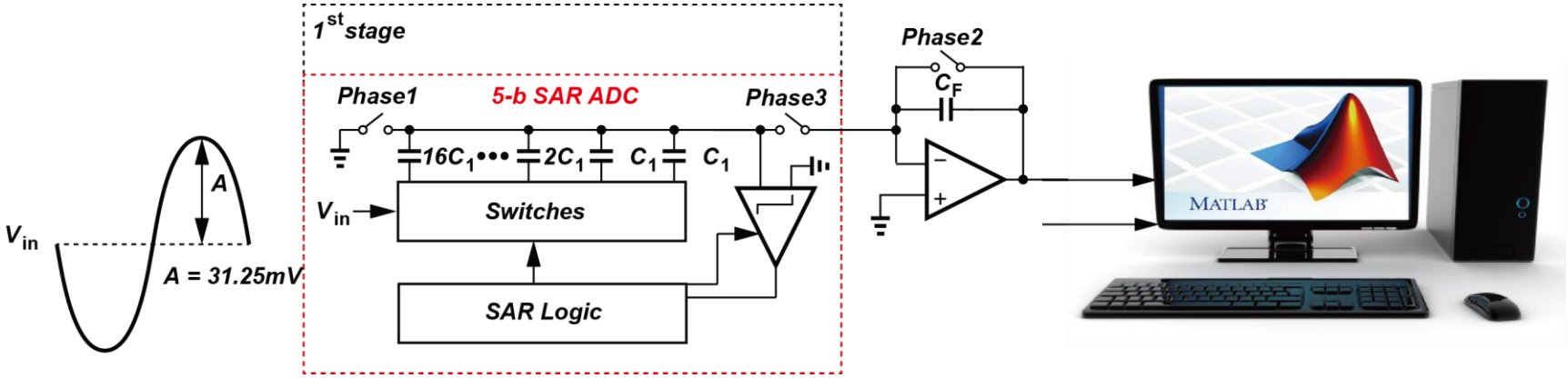
  PSD from the output of amplifer shows the SFDR is 78 dB .

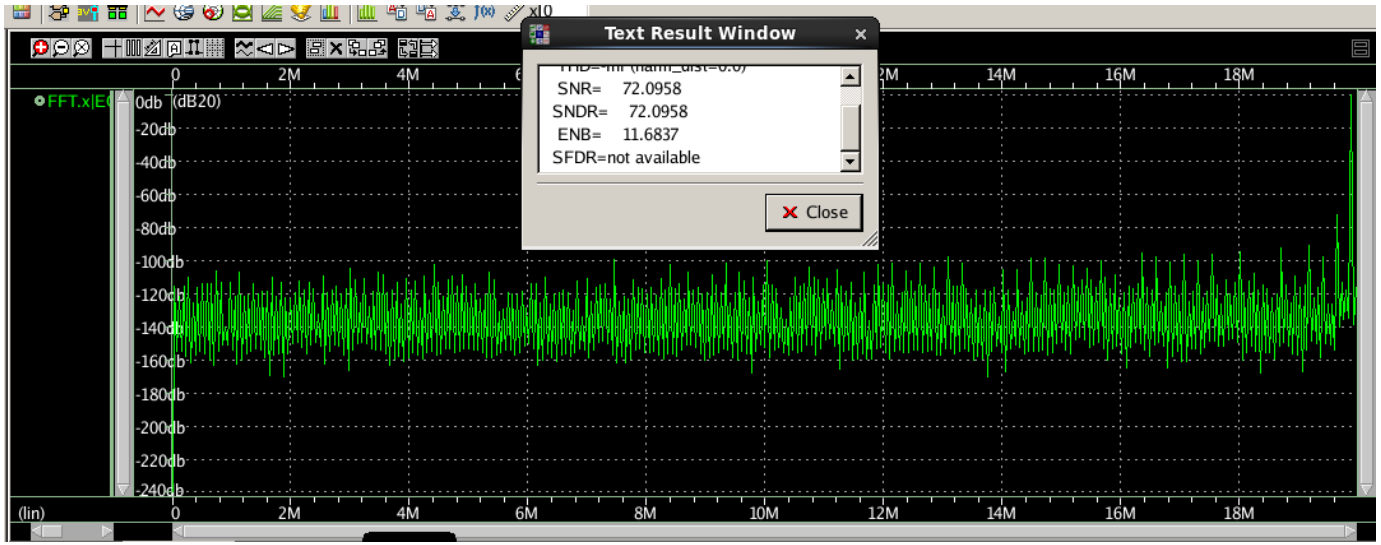
- 12-b Dynamic Performance

  Resut:

  The SFDR is better than 90 dB.

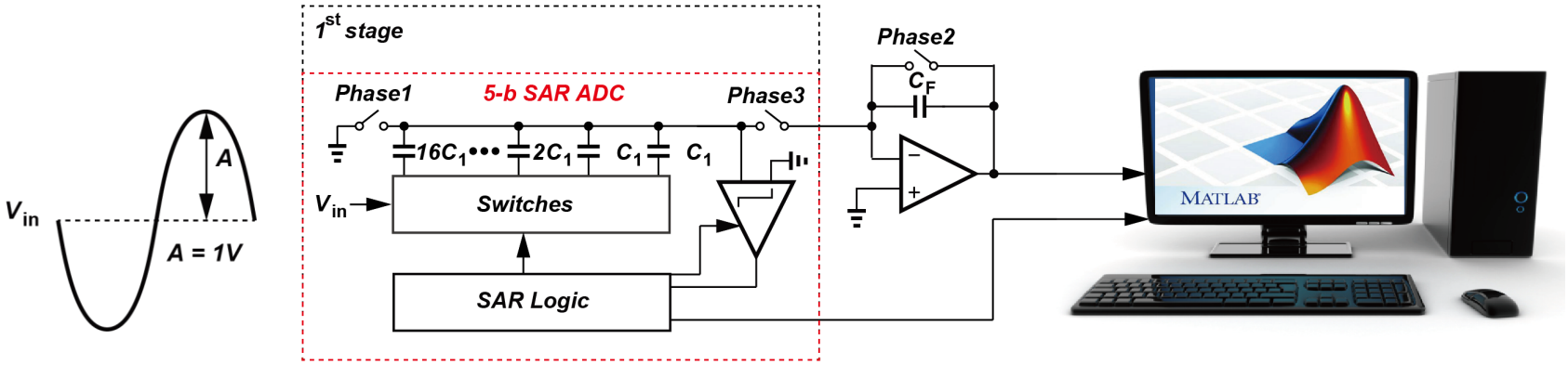
Amplifier Linearity test

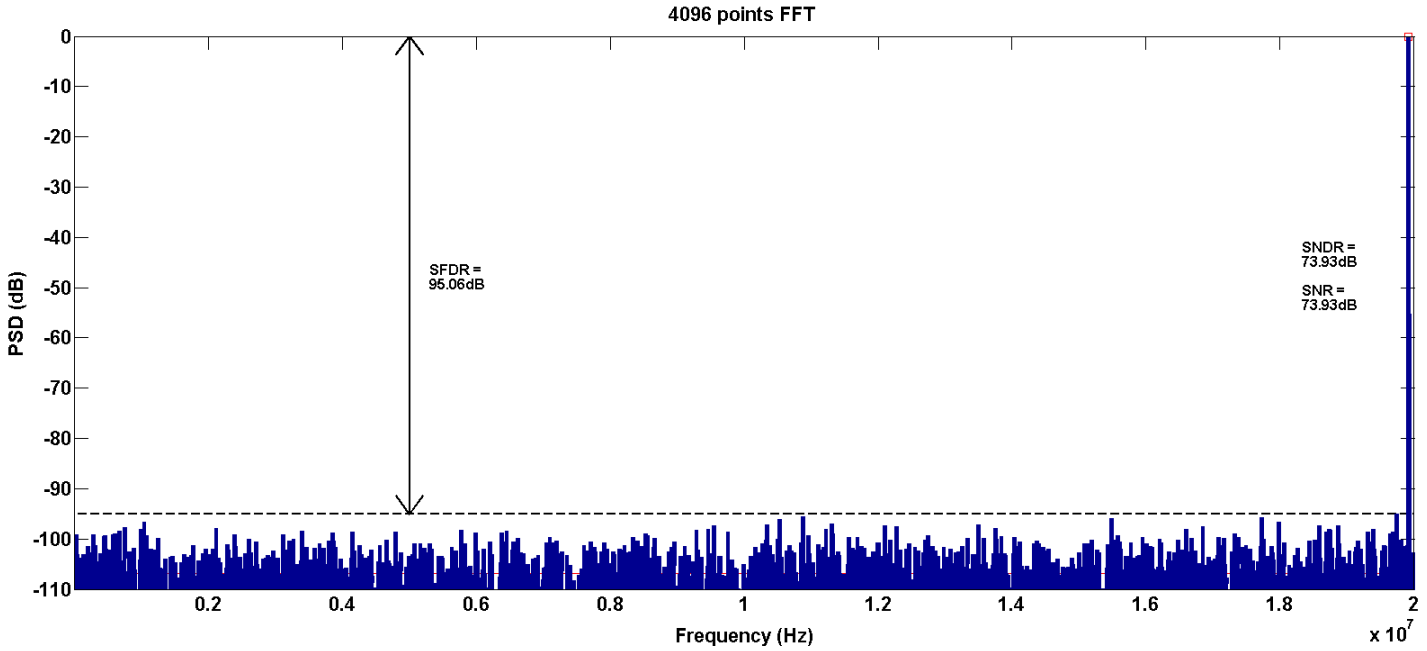




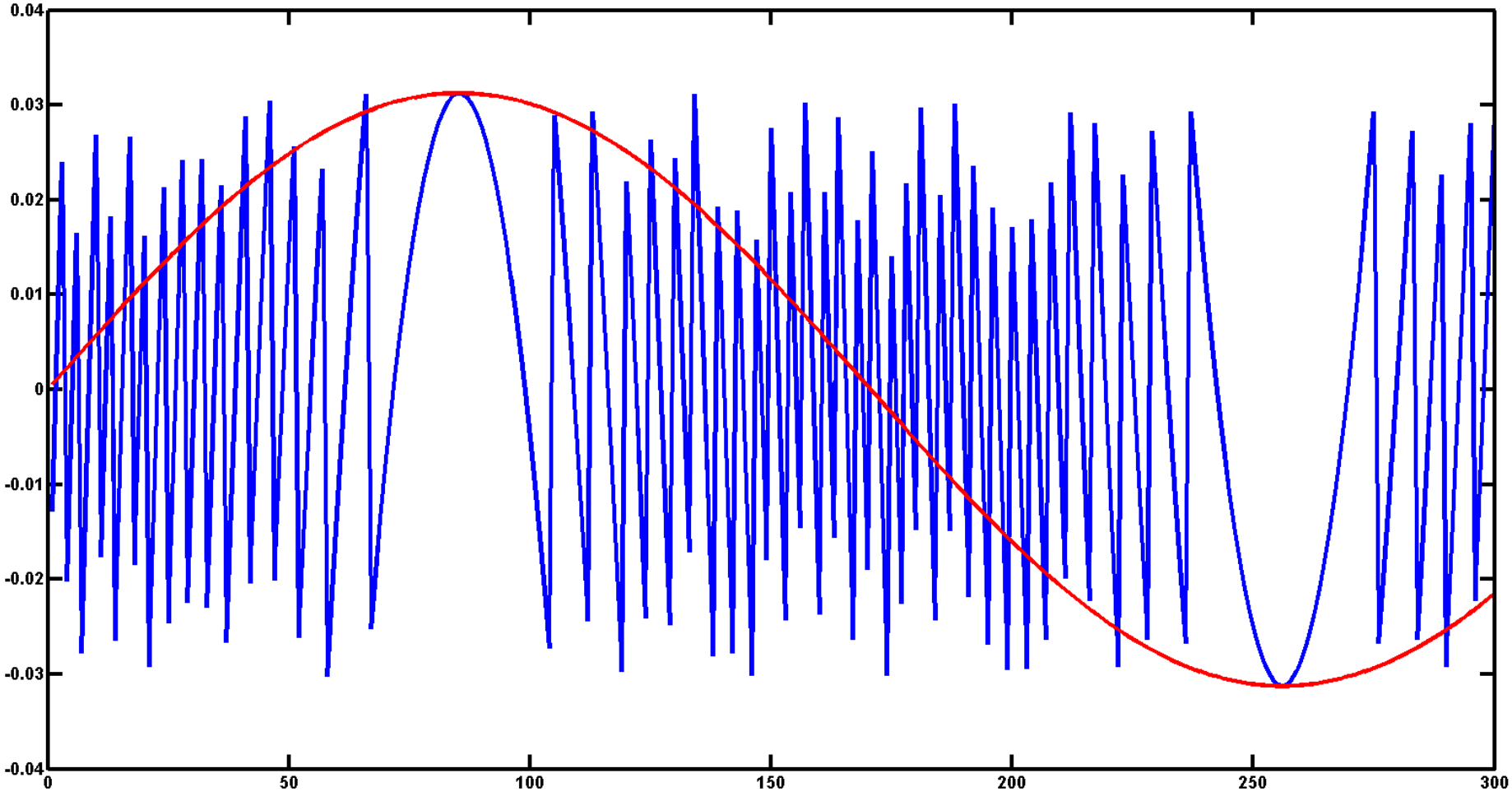
12-b Dynamic Performance

- Feed the residue of amplifier and digital code into Matlab.

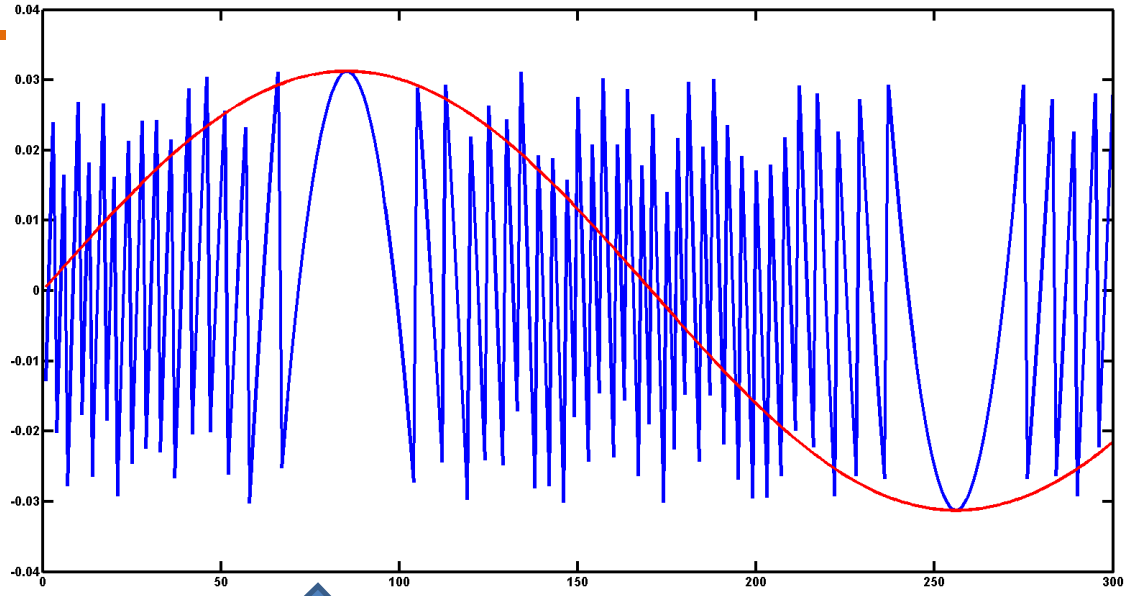


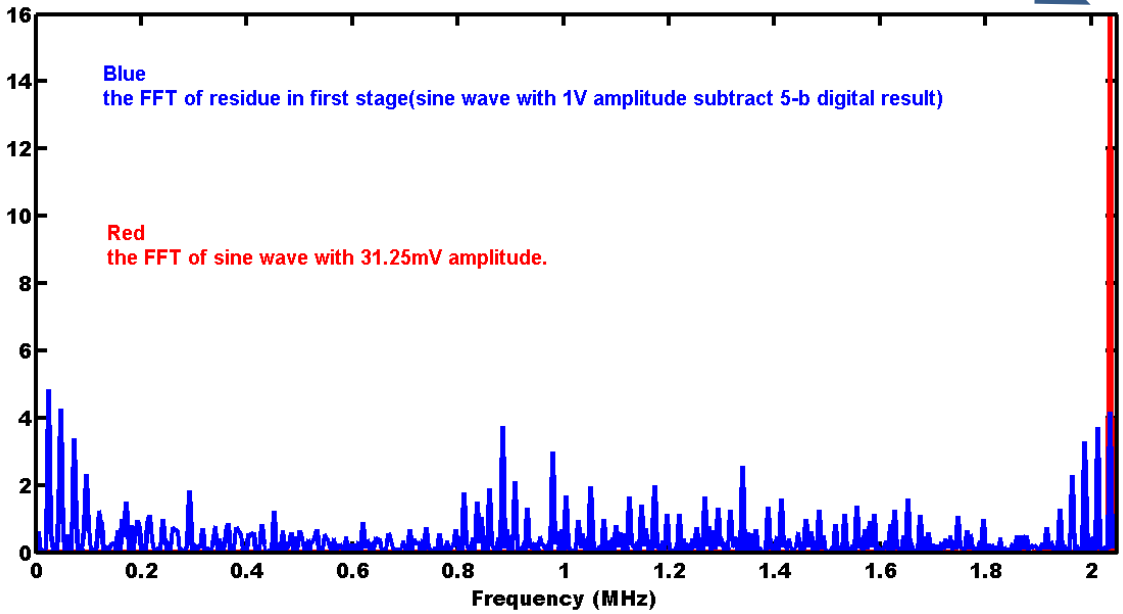


Waveform before amplifying

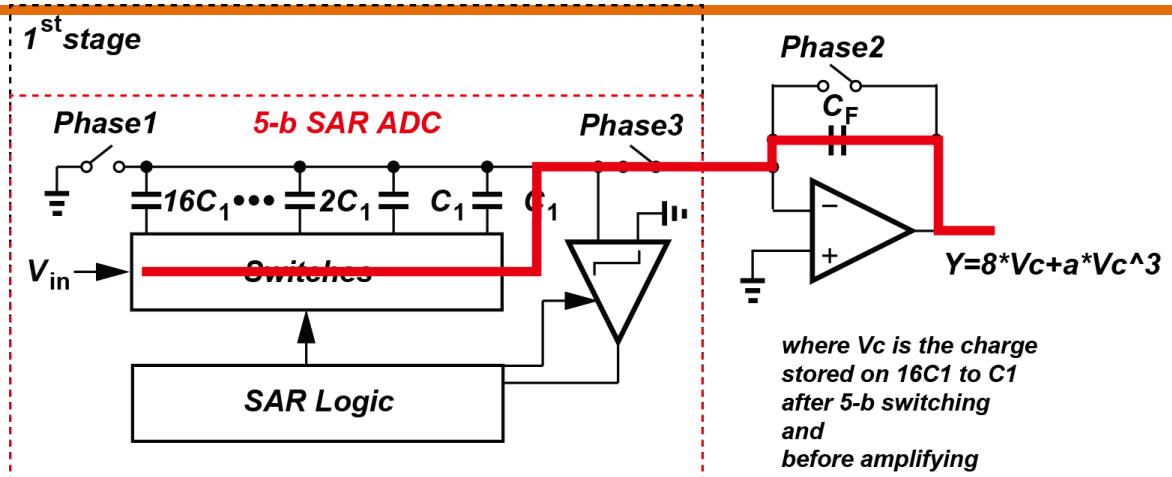


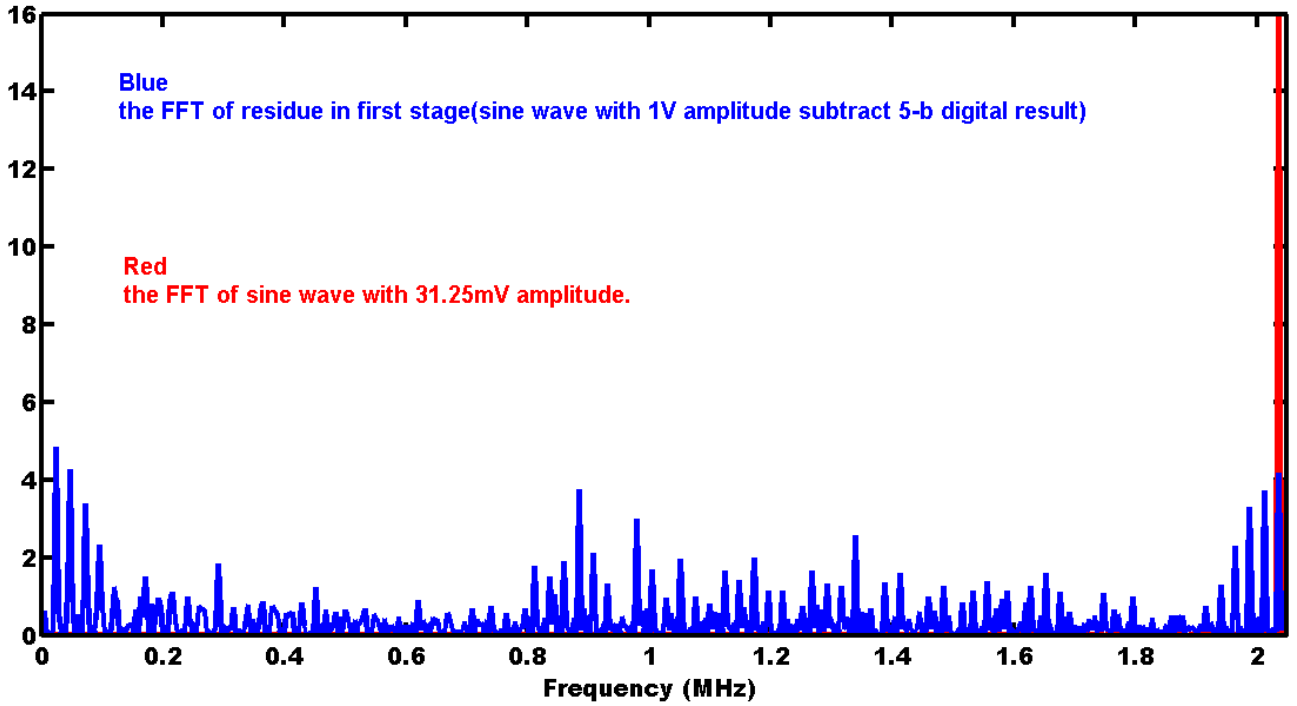
Possible Explanation





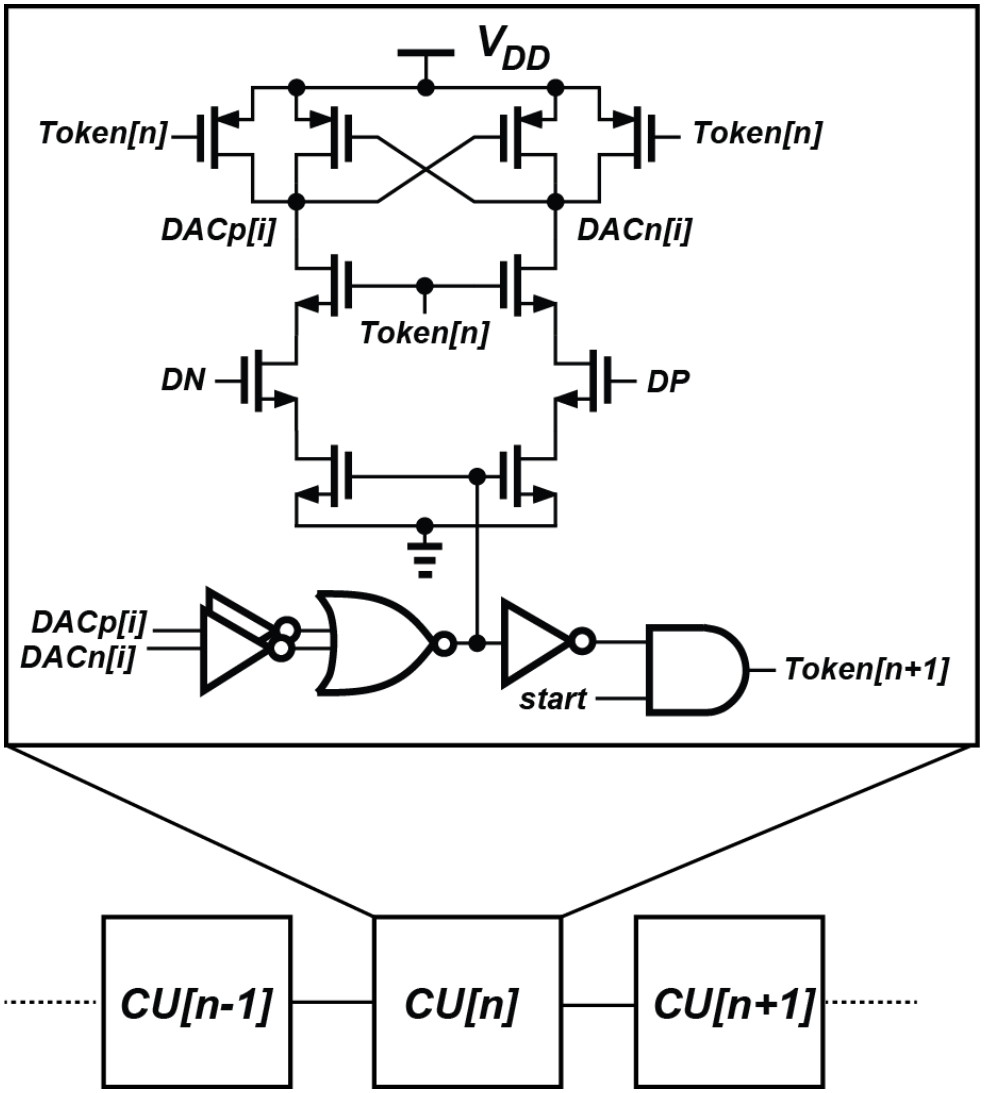
Possible Explanation





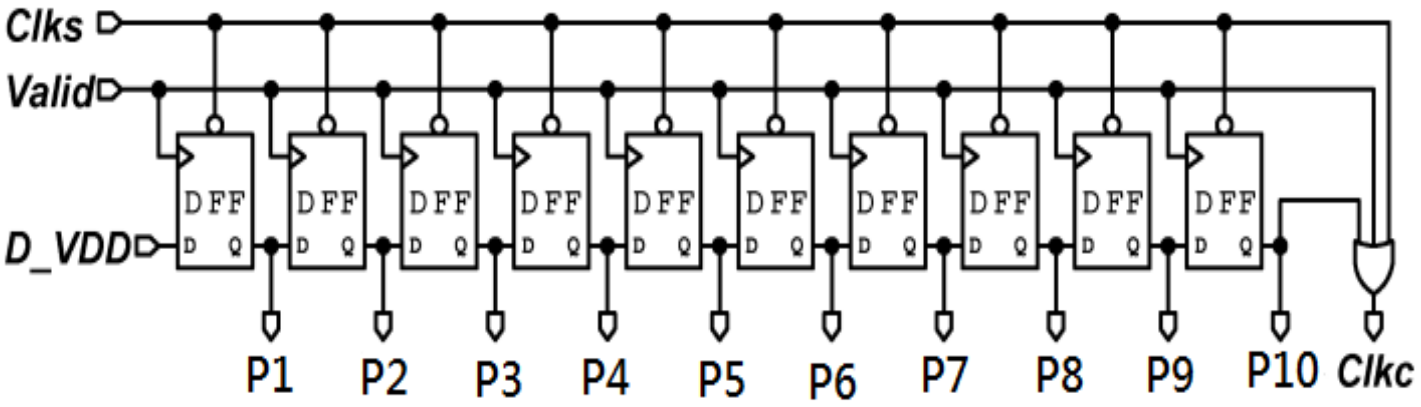
SAR Logic redesign

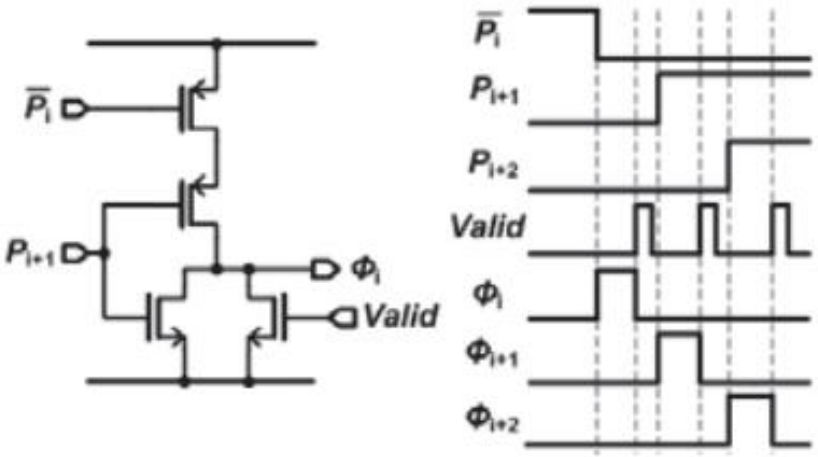
- [1] VLSI'11



SAR Logic redesign

- [2] ASSCC'13





OPAMP Corner

- Most of corners meet our requirement.

C0_0	C0_1	C0_2	C0_3	C0_4	C0_5	C0_6	C0_7
TT	TT	TT	TT	TT	TT	TT	TT
1.08	1.08	1.08	1.2	1.2	1.2	1.32	1.32
-20	27	80	-20	27	80	-20	27

C0_0	C0_1	C0_2	C0_3	C0_4	C0_5	C0_6	C0_7
3.291G	2.83G	2.425G	3.408G	3.015G	2.643G	3.53G	3.151G
81.96	81.32	75.74	90.93	88	82.83	93.39	88.32

C0_27	C0_28	C0_29	C0_30	C0_31	C0_32	C0_33	C0_34	C0_35
FS	FS	FS	FS	FS	FS	FS	FS	FS
1.08	1.08	1.08	1.2	1.2	1.2	1.32	1.32	1.32
-20	27	80	-20	27	80	-20	27	80

1.08
Parameter: VDD

C0_27	C0_28	C0_29	C0_30	C0_31	C0_32	C0_33	C0_34	C0_35
3.12G	2.769G	2.274G	3.427G	2.921G	2.5G	3.501G	3.055G	2.658G
33.79	81.93	72.95	88.2	85.28	79.84	90.86	85.73	81.03

C0_18	C0_19	C0_20	C0_21	C0_22	C0_23	C0_24	C0_25	C0_26
SS	SS	SS	SS	SS	SS	SS	SS	SS
1.08	1.08	1.08	1.2	1.2	1.2	1.32	1.32	1.32
-20	27	80	-20	27	80	-20	27	80

C0_18	C0_19	C0_20	C0_21	C0_22	C0_23	C0_24	C0_25	C0_26
3.084G	2.878G	2.329G	3.055G	3.023G	2.604G	3.213G	3.147G	2.742G
33.75	81.55	76.65	53.99	90.9	85.98	61.82	92.34	86.83

C0_36	C0_37	C0_38	C0_39	C0_40	C0_41	C0_42	C0_43	C0_44
SF	SF	SF	SF	SF	SF	SF	SF	SF
1.08	1.08	1.08	1.2	1.2	1.2	1.32	1.32	1.32
-20	27	80	-20	27	80	-20	27	80

C0_36	C0_37	C0_38	C0_39	C0_40	C0_41	C0_42	C0_43	C0_44
2.901G	2.904G	2.577G	3.016G	3.098G	2.763G	3.244G	3.24G	2.899G
36.44	79.3	76.38	32.43	88.03	84.2	64.74	89.4	84.92

C0_9	C0_10	C0_11	C0_12	C0_13	C0_14	C0_15	C0_16	C0_17
FF	FF	FF	FF	FF	FF	FF	FF	FF
1.08	1.08	1.08	1.2	1.2	1.2	1.32	1.32	1.32
-20	27	80	-20	27	80	-20	27	80

C0_9	C0_10	C0_11	C0_12	C0_13	C0_14	C0_15	C0_16	C0_17
3.226G	2.835G	2.482G	3.395G	3.026G	2.675G	3.535G	3.175G	2.823G
83.5	79.3	70.98	88.59	83.34	77.66	88.83	84.09	78.85

Reference

1. J.-H. Tsai, Y.-J. Chen, M.-H. Shen and P.-C. Huang, “A 1-V, 8b, 40MS/s, 113µW Charge-Recycling SAR ADC with a 14µW Asynchronous Controller,” ***Symp. on VLSI Circuits***, pp. 264-265, June 2011.
2. G. Y. Huang, S. J. Chang, Y. Z. Lin, C. C. Liu and C. P. Huang, “A 10b 200MS/s 0.82mW SAR ADC in 40nm” in Proc. ***IEEE A-SSCC***, pp. 289-292, 2013.

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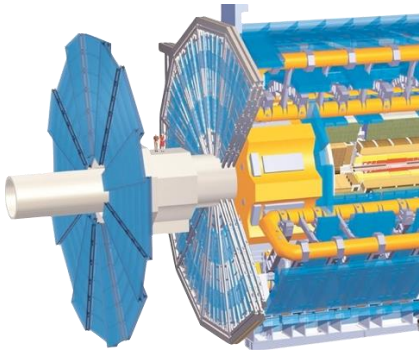

UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

Chen-Kai Hsu

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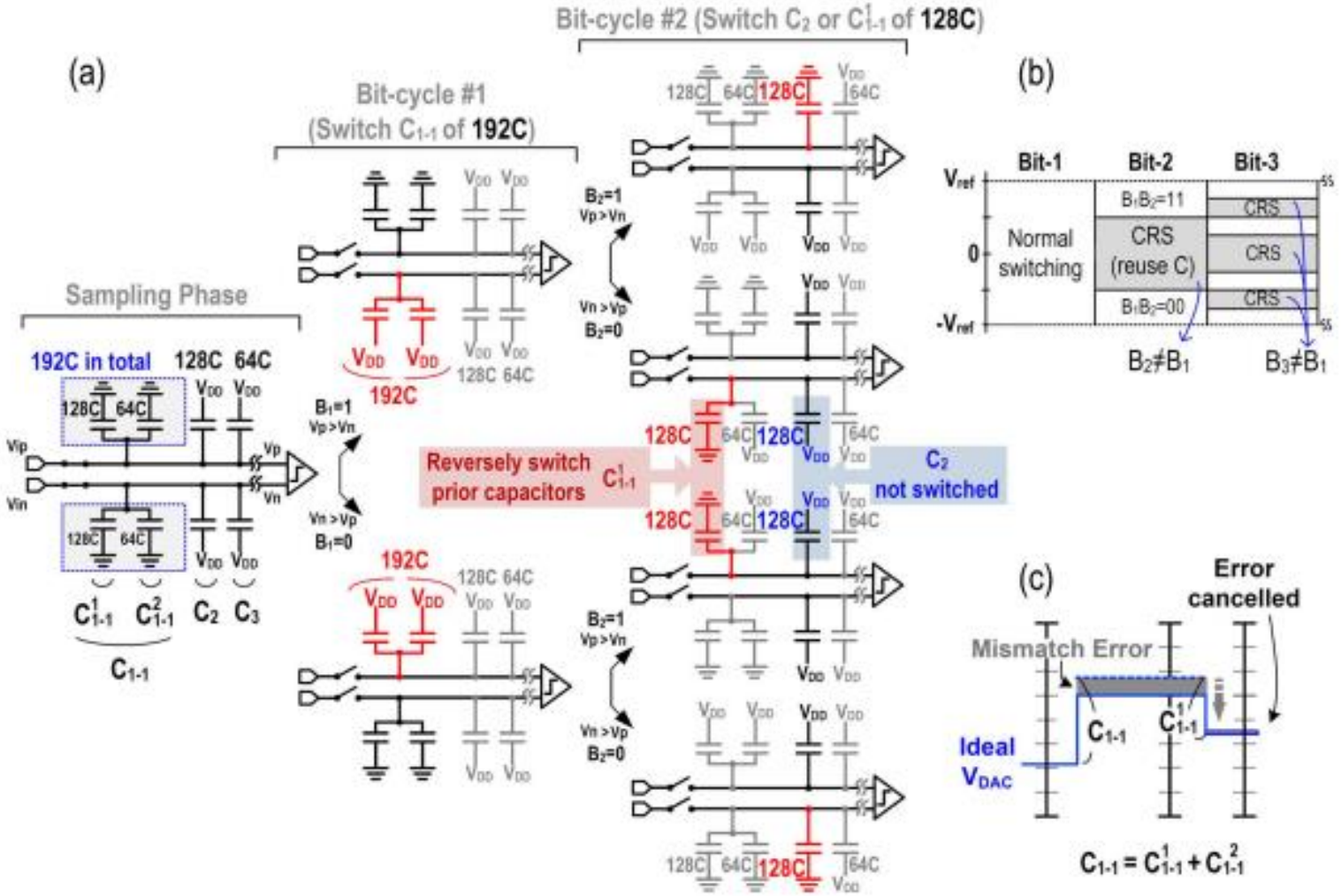
Nov 22, 2016

Outline

- Capacitor Linearity Enhancement
- Implementation Progress
- Future work

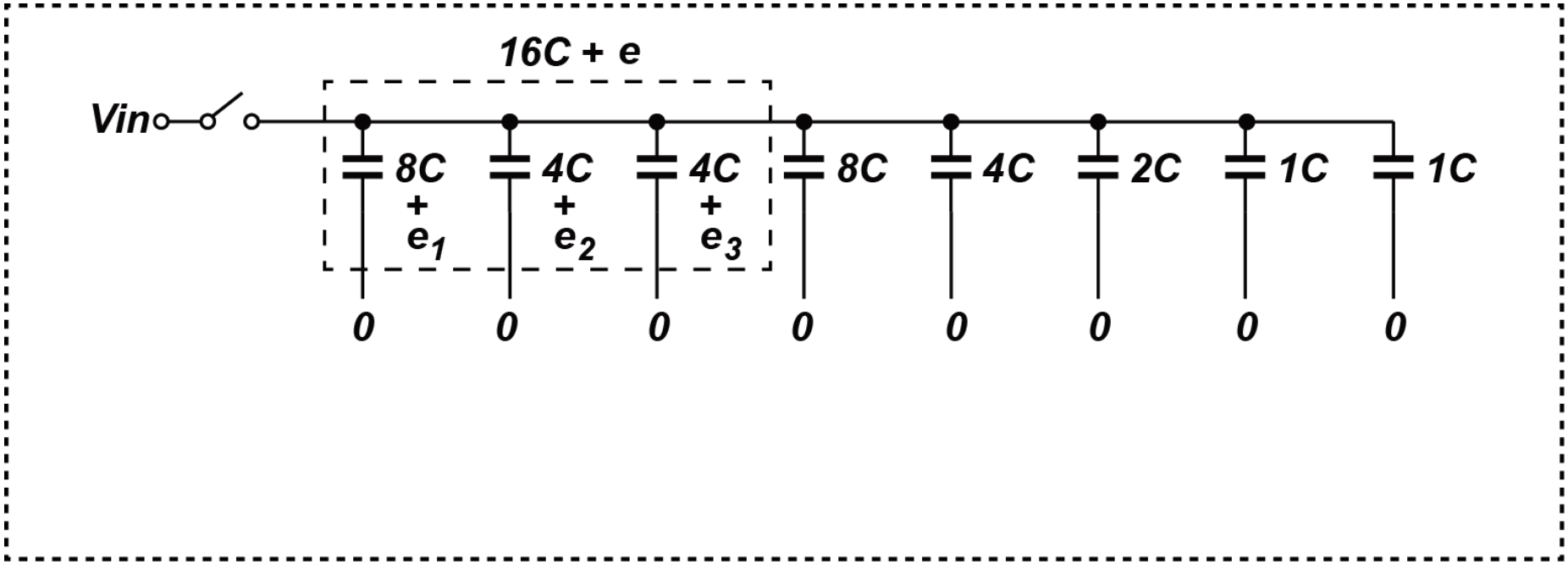
Capacitor Matching Enhancement

- Reversed Switching, RS, [1] JSSCC'15



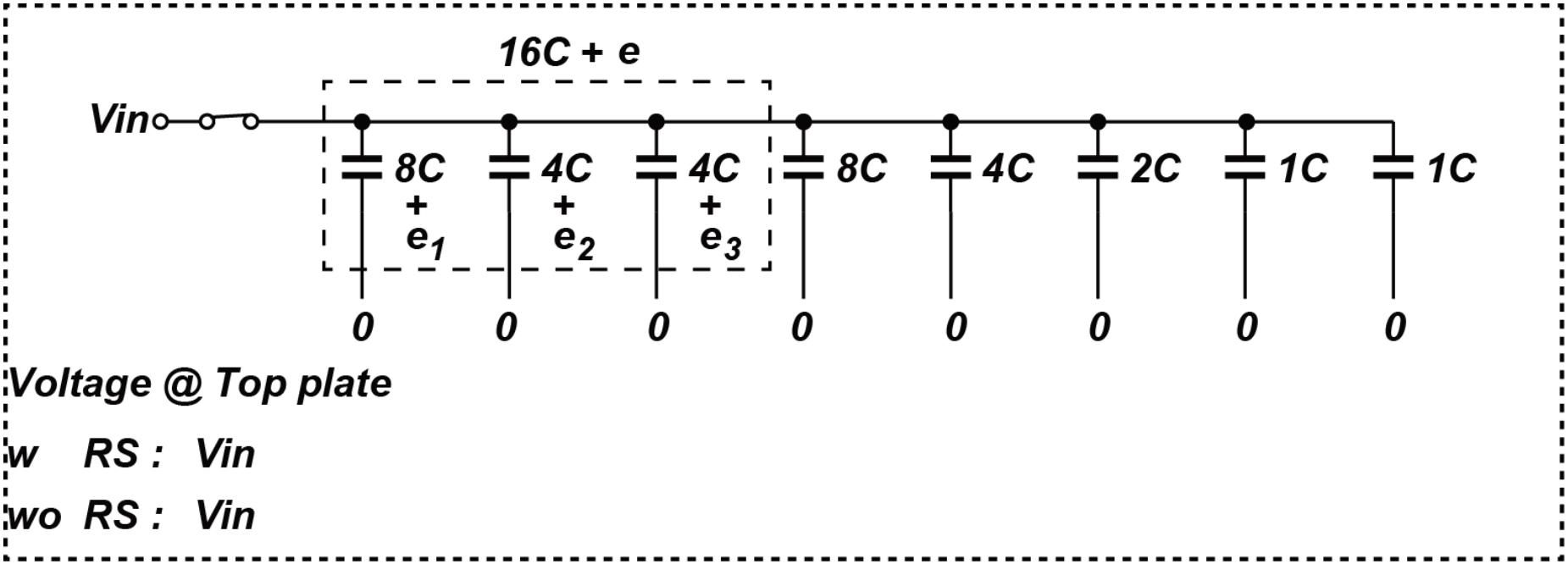
Capacitor Matching Enhancement

- Digital Sequence : 100



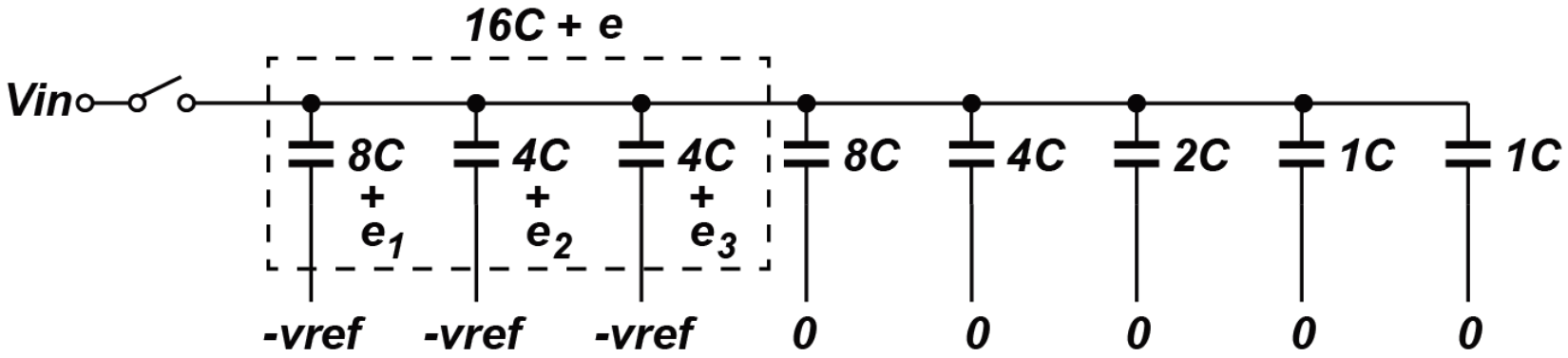
Capacitor Matching Enhancement

- Digital Sequence : 100



Capacitor Matching Enhancement

- Digital Sequence : 100



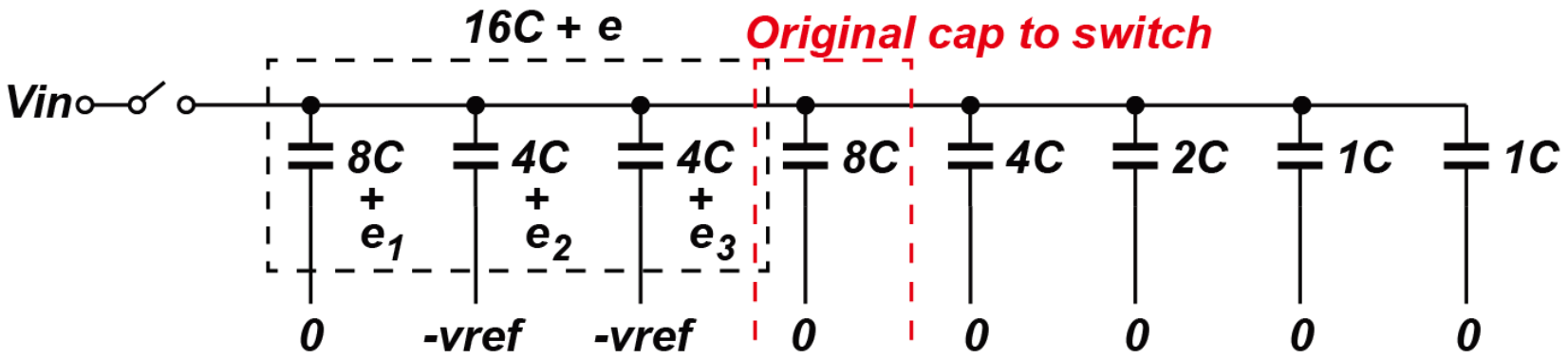
Voltage @ Top plate

*w RS : Vin-((16c+e)/(32c+e))*vref*

*wo RS : Vin-((16c+e)/(32c+e))*vref*

Capacitor Matching Enhancement

- Digital Sequence : 100



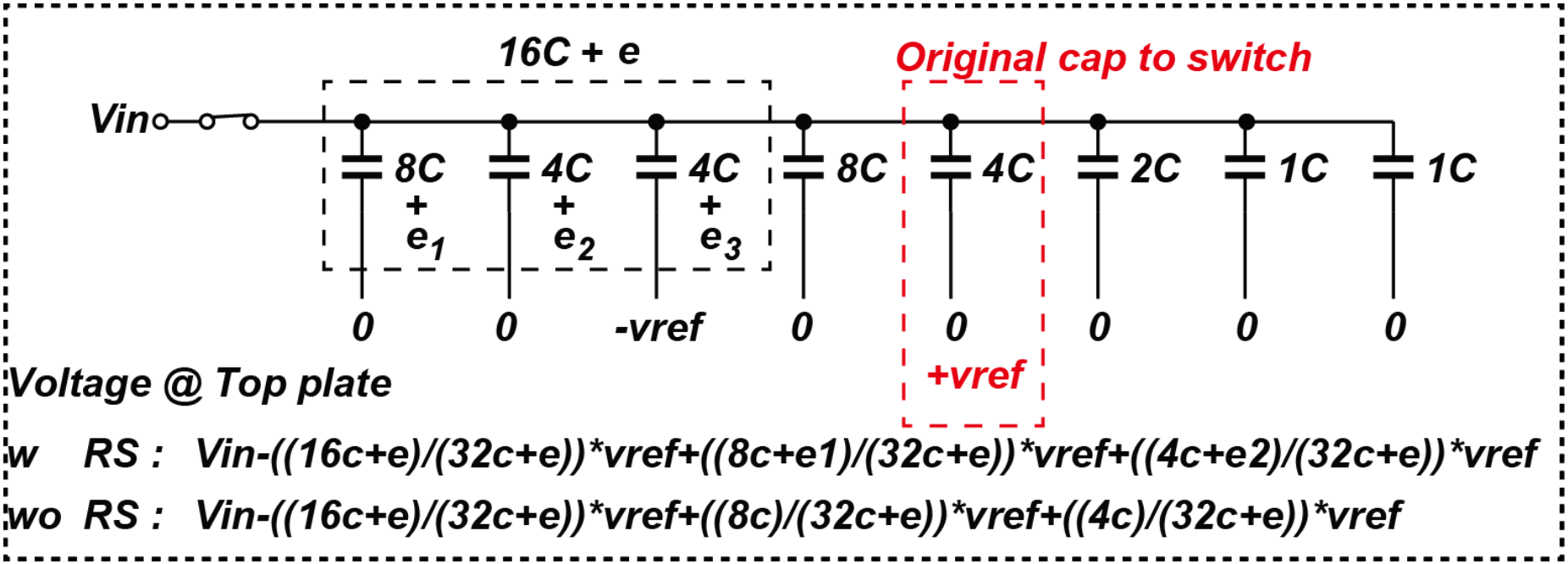
Voltage @ Top plate

w RS : Vin-((16c+e)/(32c+e))*vref+((8c+e1)/(32c+e))*vref

wo RS : Vin-((16c+e)/(32c+e))*vref+((8c)/(32c+e))*vref

Capacitor Matching Enhancement

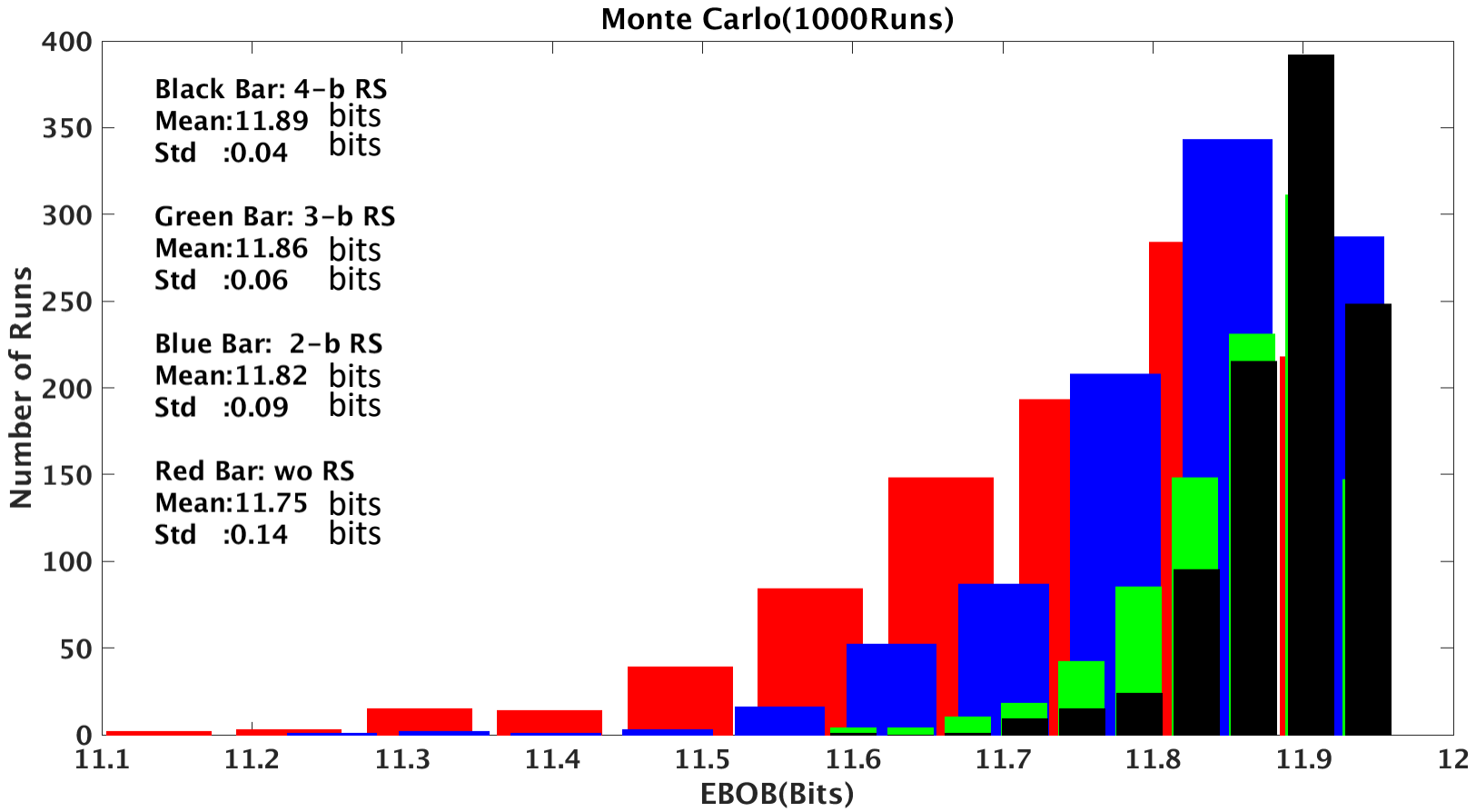
- Digital Sequence : 100



- Remember that e equals to e1+e2+e3

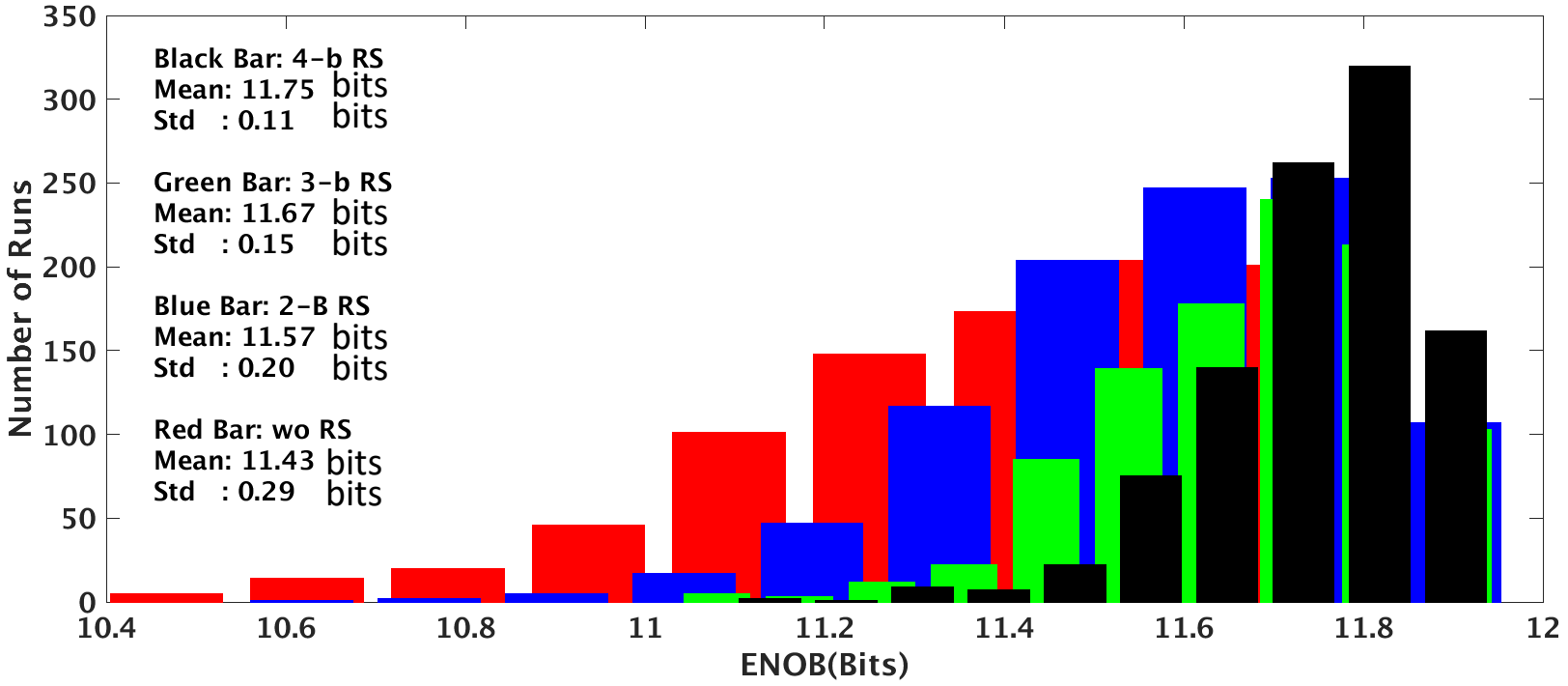
Capacitor Matching Enhancement

- Unit capacitor of 200fF in 1st stage.



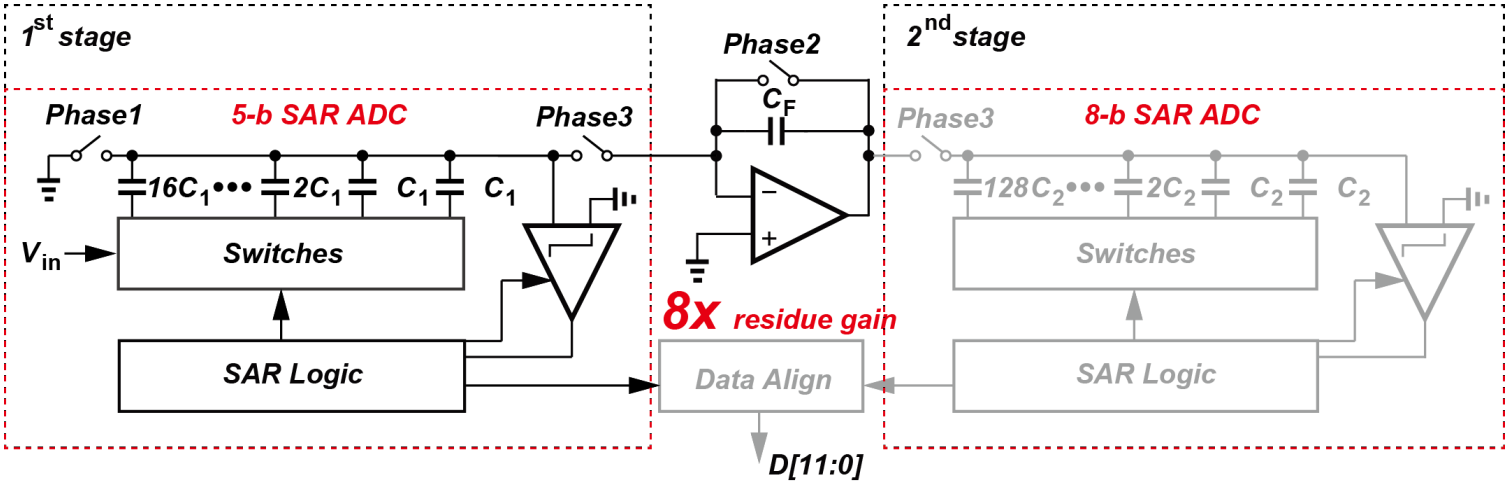
Capacitor Matching Enhancement

- Unit capacitor of 20fF in 1st stage.



Implementation Progress

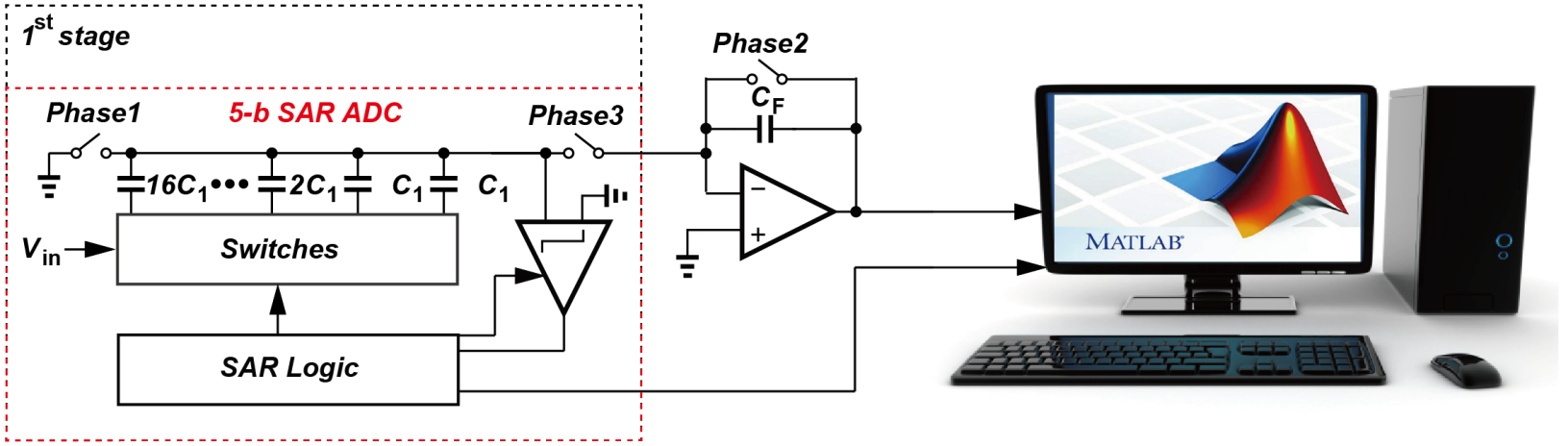
- First stage has been built(without RS).

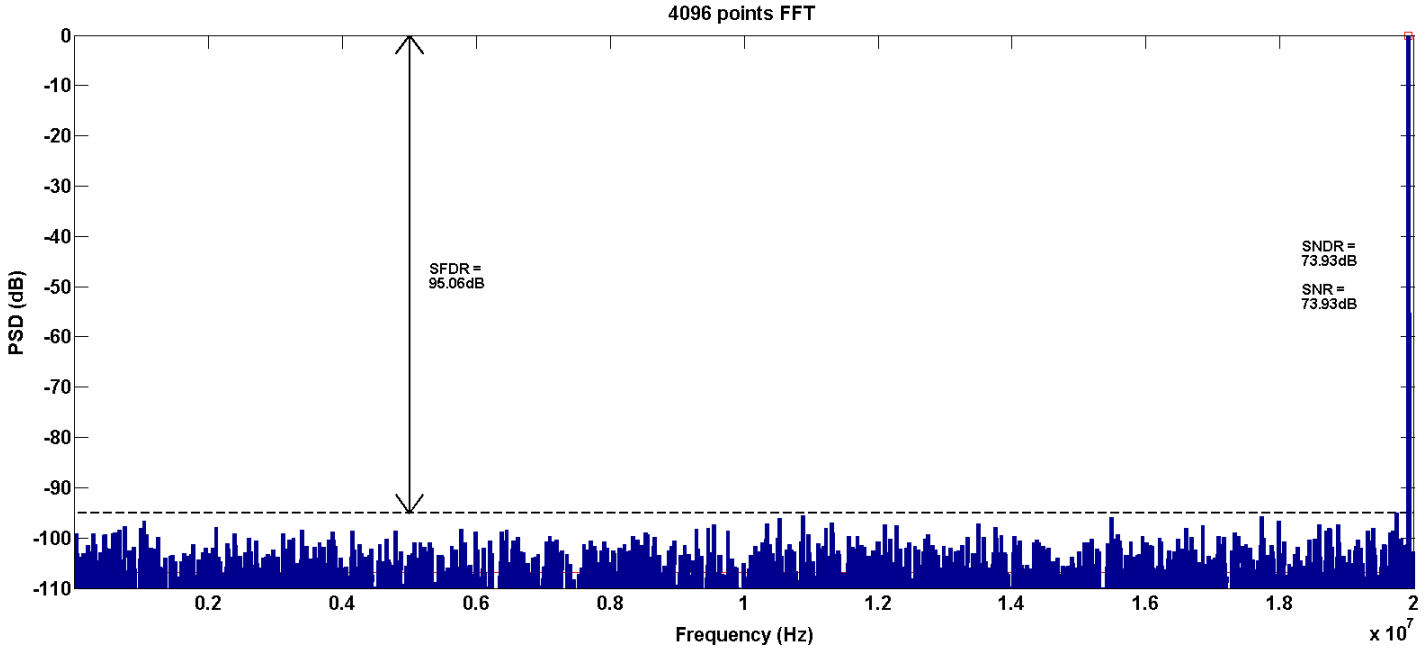


	Power Consumption
OPAMP	1.8mW
1st Comparator	60uW
1st SAR Logic	20uW
Bootstrap Switch	6uW

Implementation Progress

- Feed the residue of amplifier and digital code into Matlab.





Future Work

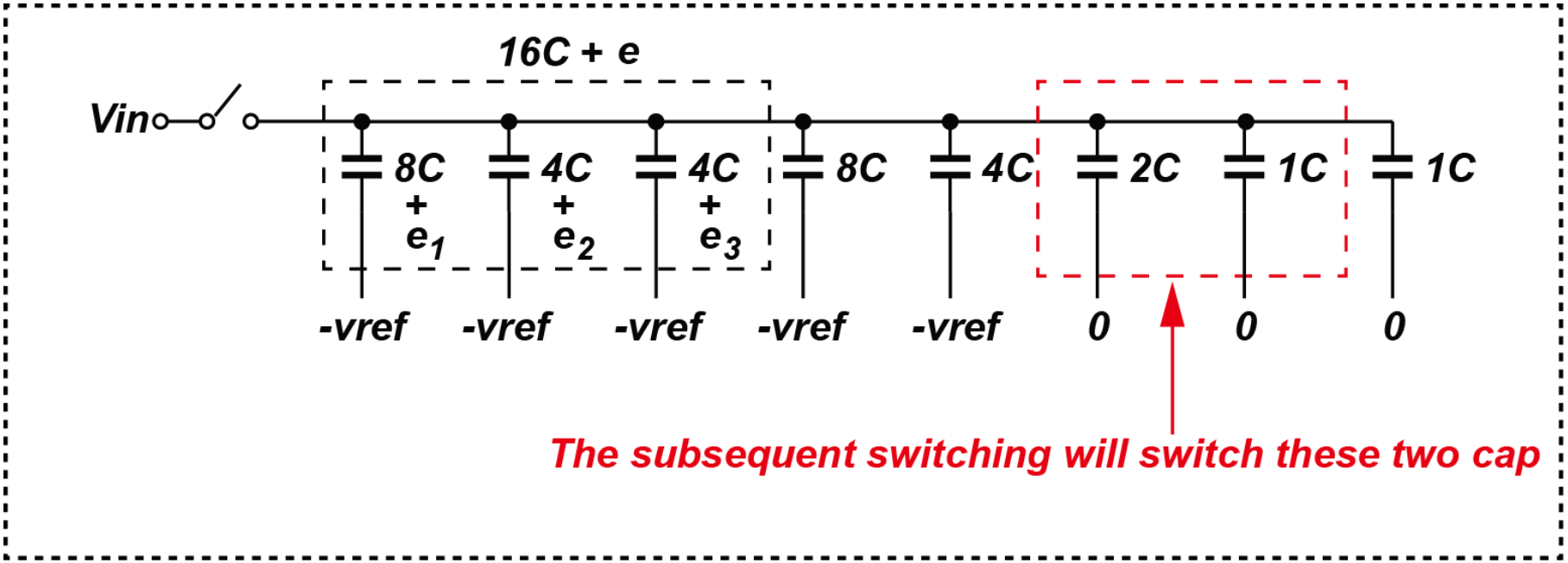
- Implement the RS technique into the first stage.
- Doing more simulation on first stage before next meeting, such as corner simulation and noise simulation.

Reference

1. J.-H. Tsai et al., “A 0.003 mm2 10 b 240 MS/s 0.7 mW SAR ADC in 28 nm CMOS with digital error correction and correlated-reversed switching,” IEEE J. Solid-State Circuits, vol. 50, no. 6, pp. 1382–1398, Jun. 2015.

Backup

If the digitized code is 111, the following switching will not switch back.

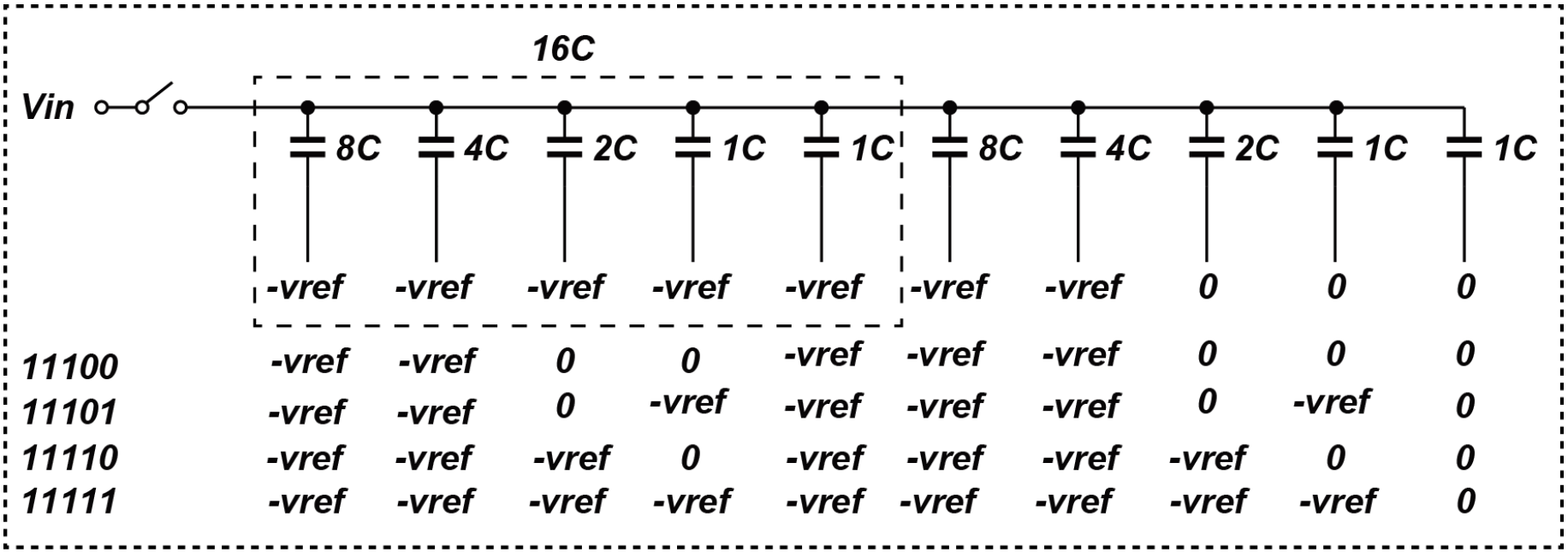


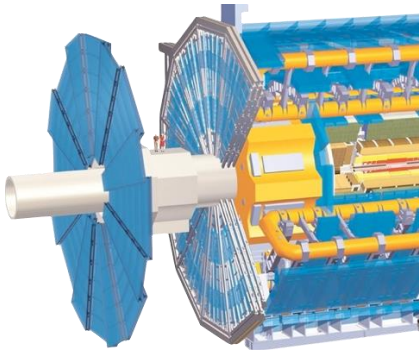
Backup

Performing more bits RS will alleviate this dilemma.

Assuming 111 has been resolved and the following sequence will be 00, 01, 10, 11.

Except for 11111, the other sequence will have at least one switching back.





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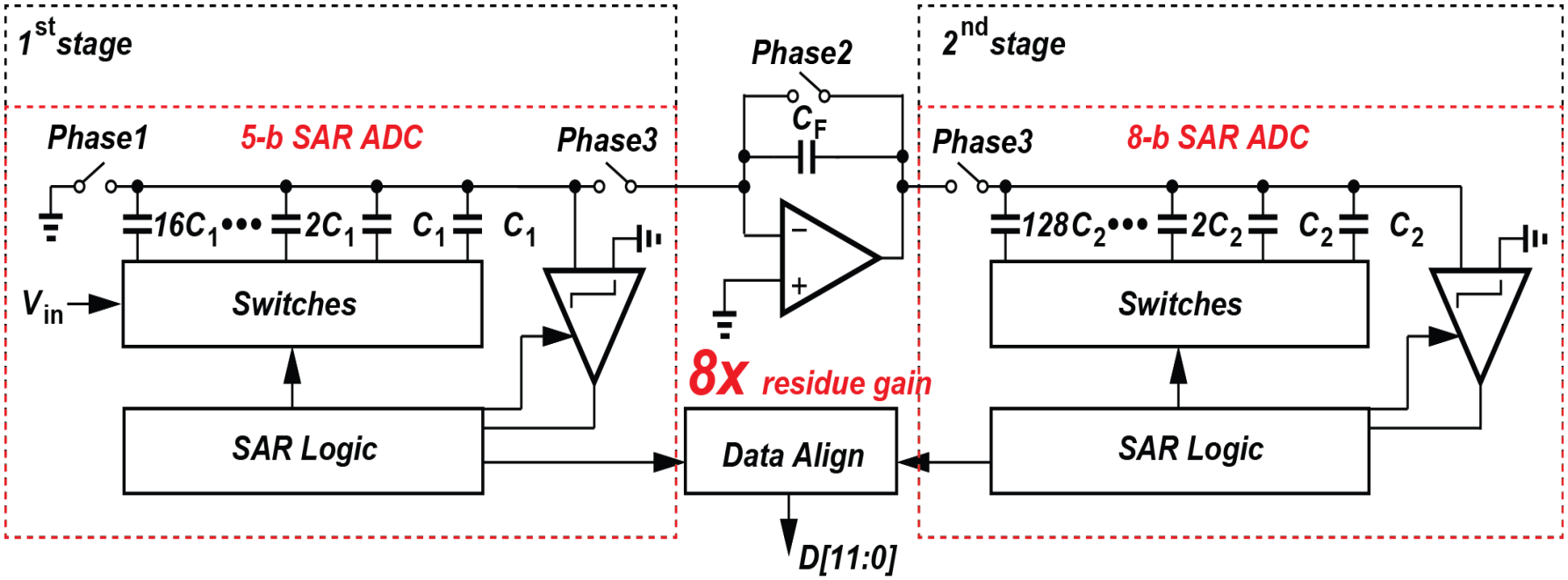
Nov 4, 2016

What about 8x inter-stage gain ?

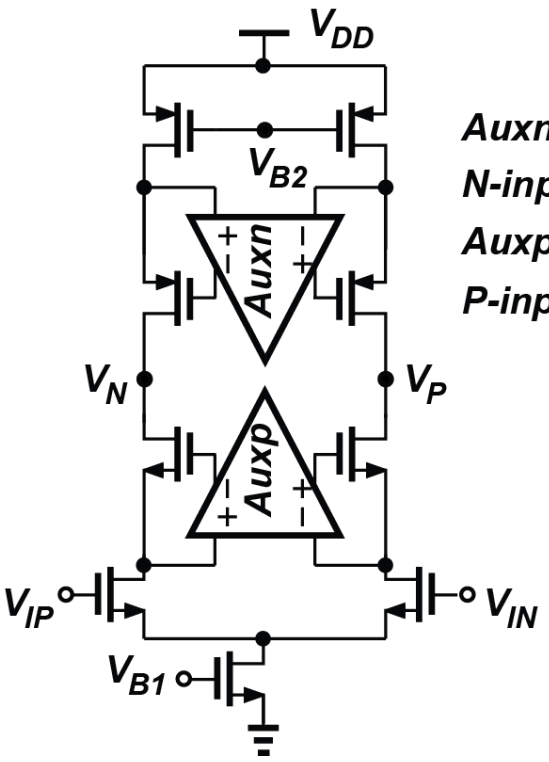


Open-Loop Gain can be reduced from 78dB to 72dB.

Unit-Gain Bandwidth can be reduced from 1.27GHz to 635MHz.

Due to reduced swing, maybe we can just use telescopic with gain boosting(One-stage which means low power).

OPAMP

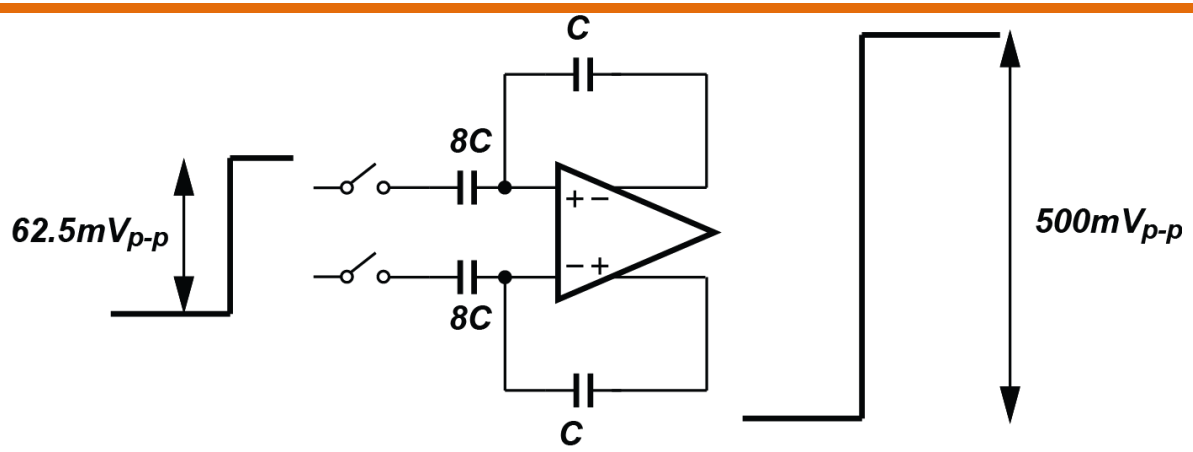


Auxn:
N-input Folded Cascode
Auxp:
P-input Folded Cascode

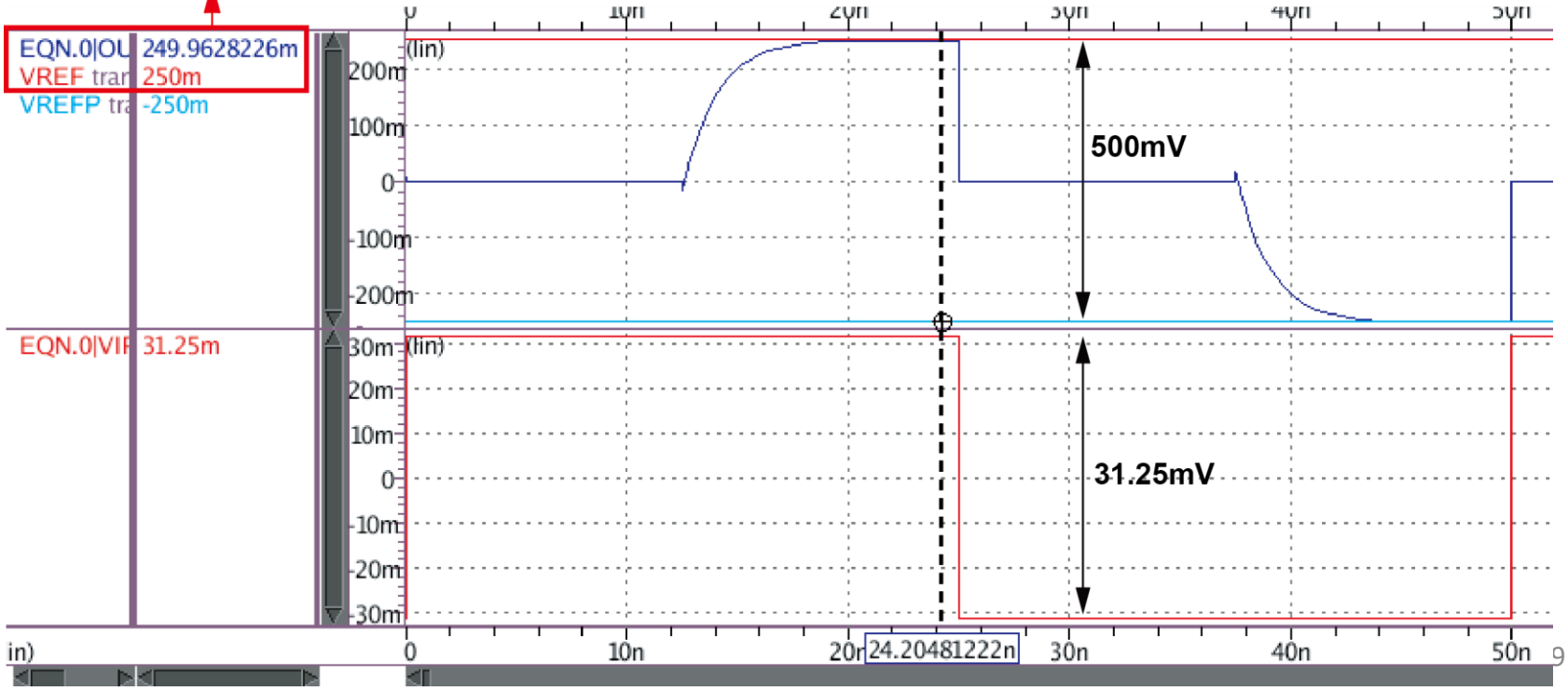
	Specification
Supply Voltage	1.2 V
Technology	TSMC 65LP 1P6M
DC Gain	80dB
Current-Main	750uA
Current-Auxn	100uA
Current-Auxp	100uA
Bias Circuit	200uA
PhaseMargin	80 degree
Unit-Gain Freq	2.1GHz

- According to [1], the frequency response of this opamp has to be carefully designed to ensure stability and to avoid pole-zero doublet, causing slow settling.
- $\beta\omega_{main,ta} < \omega_{aux,ta} < \omega_{main,2n\,pole}$

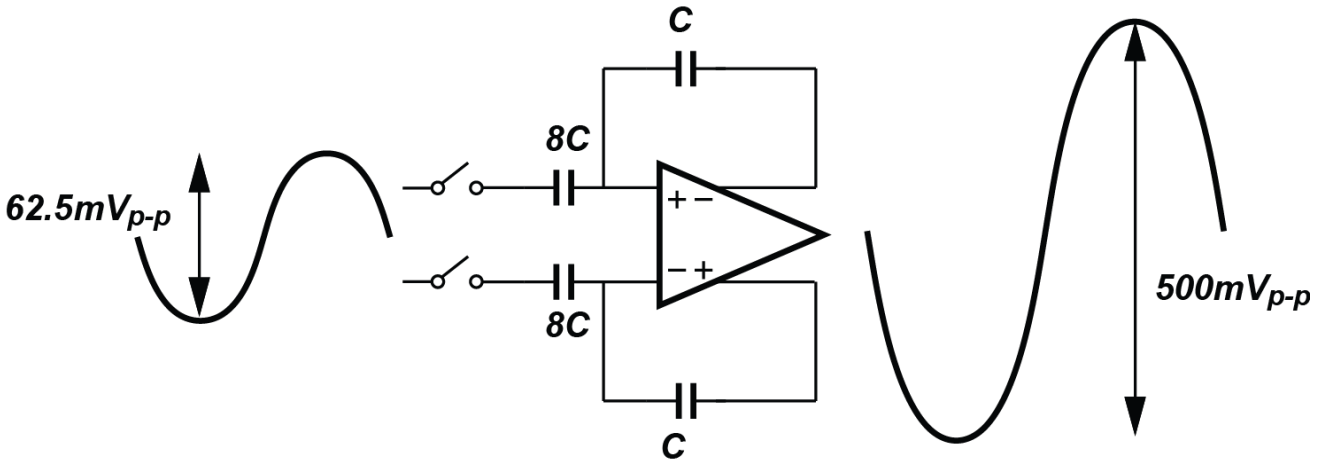
Step Response

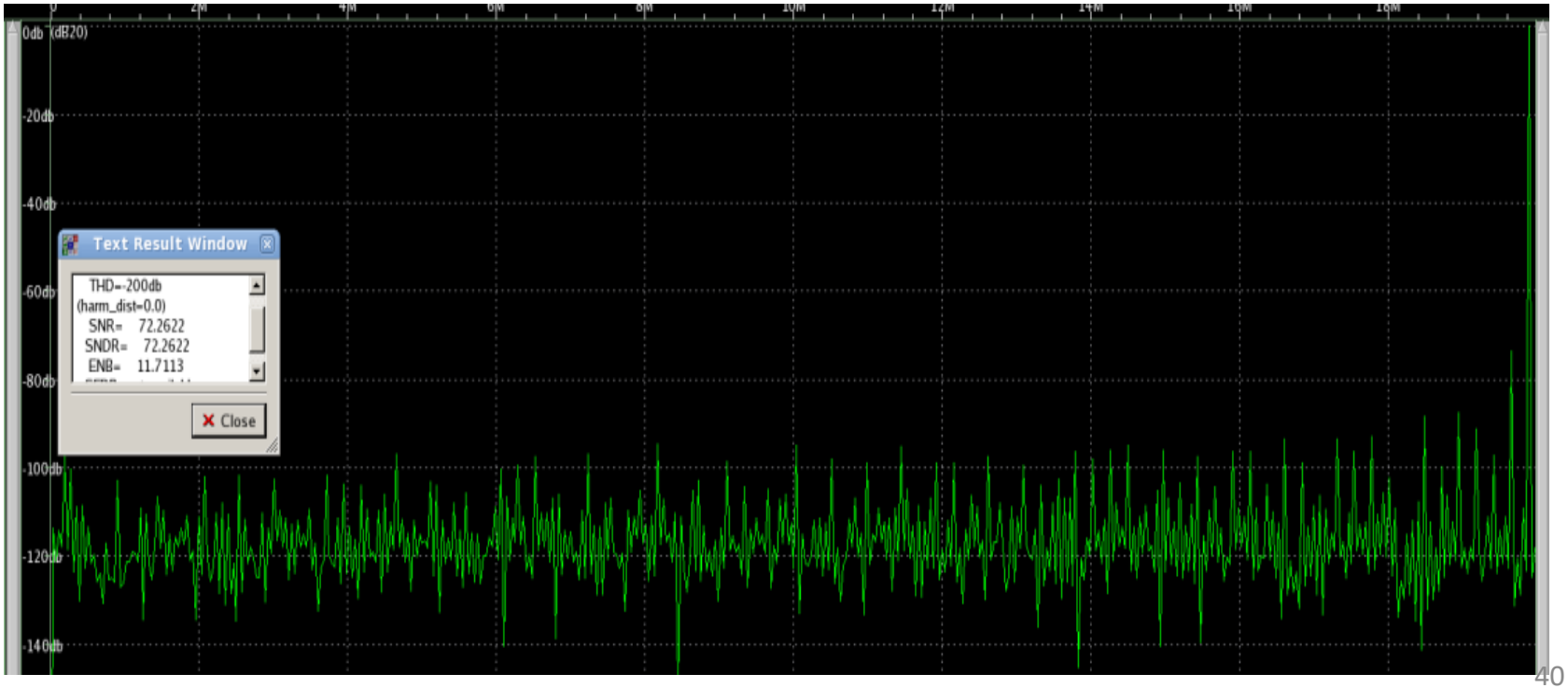


Error = 250m-249.96m = 0.04m < (0.5)/2^9



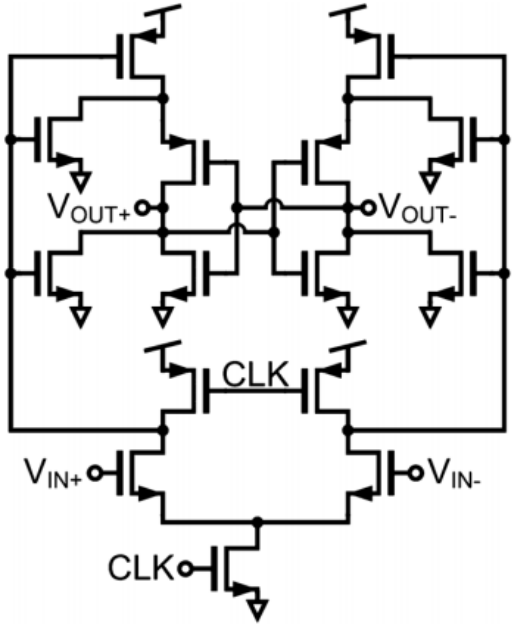
Linearity Test



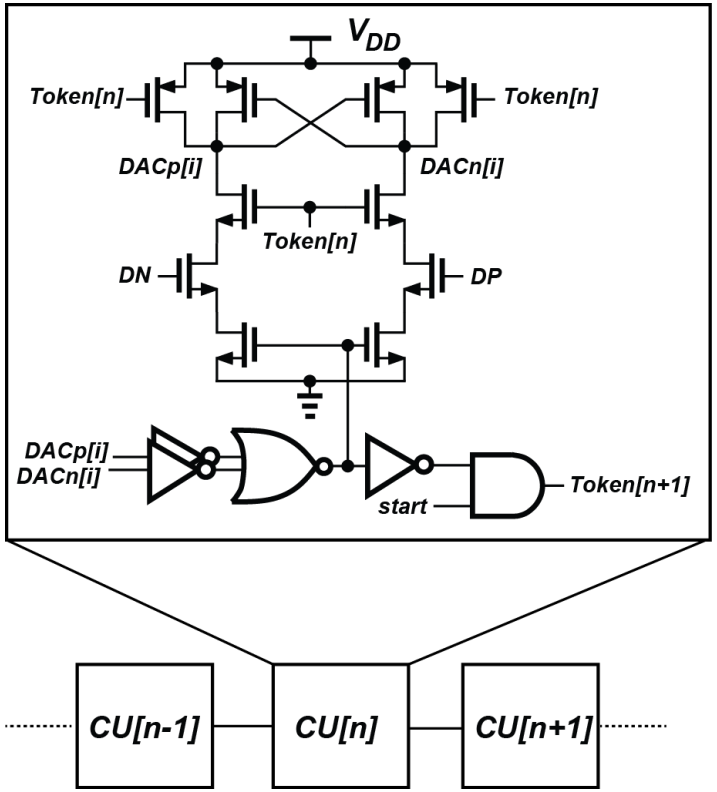


Comparator & SAR Logic

- [2] ISSCC' 15
- Low noise single phase dynamic latched comparator

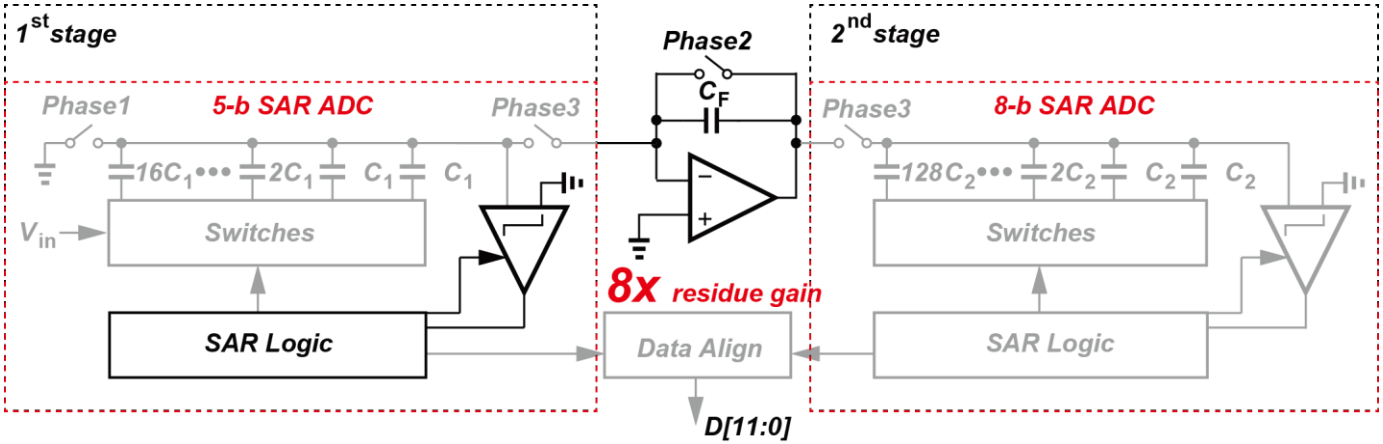


- [3] VLSI'11
- Direct switching

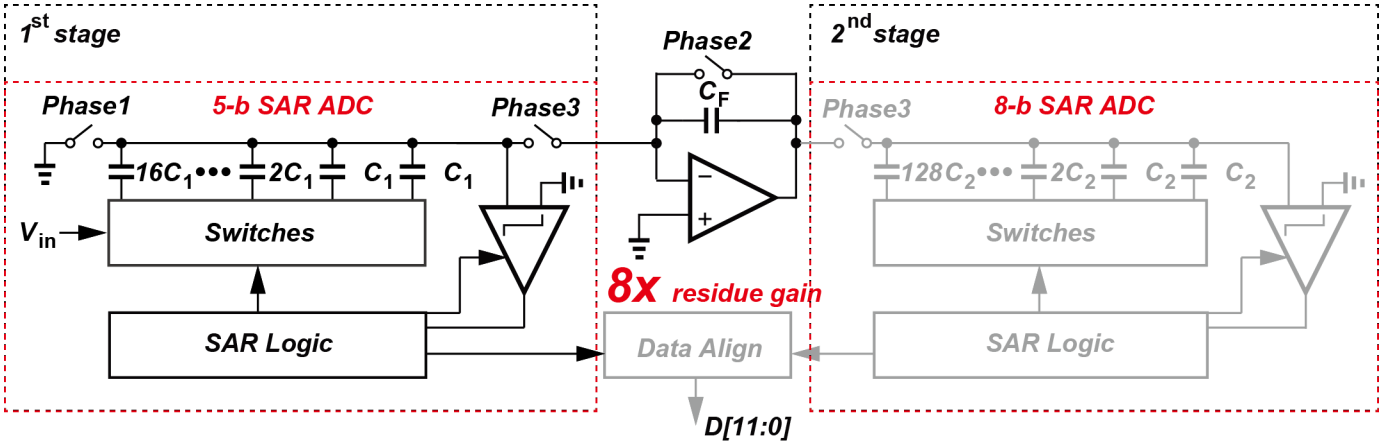


Progress

- **Things have been done:**



- **Future Plan(in the near 1 to 2 weeks):**



Some 12-b Prior Arts

	[4] ESSCIRC'16	[2] ISSCC'15
Architecture	Noise Shaping SAR ADC	Pipeline SAR ADC
Technology	130 nm	65 nm
DAC Calibration	No	No
Total capacitance	2.1 pF	2.048 pF
SNDR	74 dB	70.9 dB
SFDR	95 dB	84.6 dB

Reference

1. K. Bult and G. J. G. M. Geelen, “A fast-settling CMOS Op Amp for SC circuits with 90-dB dc gain,” ***IEEE J. Solid-State Circuits***, vol. 25, pp.1379–1384, Dec. 1990.
2. Y. Lim and M. P. Flynn, “A 1 mW 71.5 dB SNDR 50 MS/S 13b fully differential ring-amplifier-based SAR-assisted pipeline ADC,” ***in Proc. IEEE ISSCC. Dig. Tech. Papers***, Feb. 2015, pp. 1–3.
3. J.-H. Tsai, Y.-J. Chen, M.-H. Shen and P.-C. Huang, “A 1-V, 8b, 40MS/s, 113µW Charge-Recycling SAR ADC with a 14µW Asynchronous Controller,” ***Symp. on VLSI Circuits***, pp. 264-265, June 2011.
4. Wenjuan Guo, and Nan Sun , “A 12b-ENOB 61µW noise-shaping SAR ADC with a passive integrator ,” ***ESSCIRC,*** pp. 405-408, Oct. 2016.

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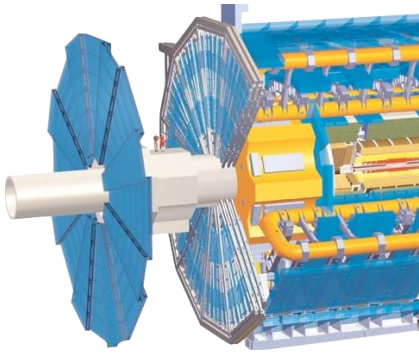

UT-Austin ADC Design ATLAS LAr Calorimeter at HL-LHC

Chen-Kai Hsu

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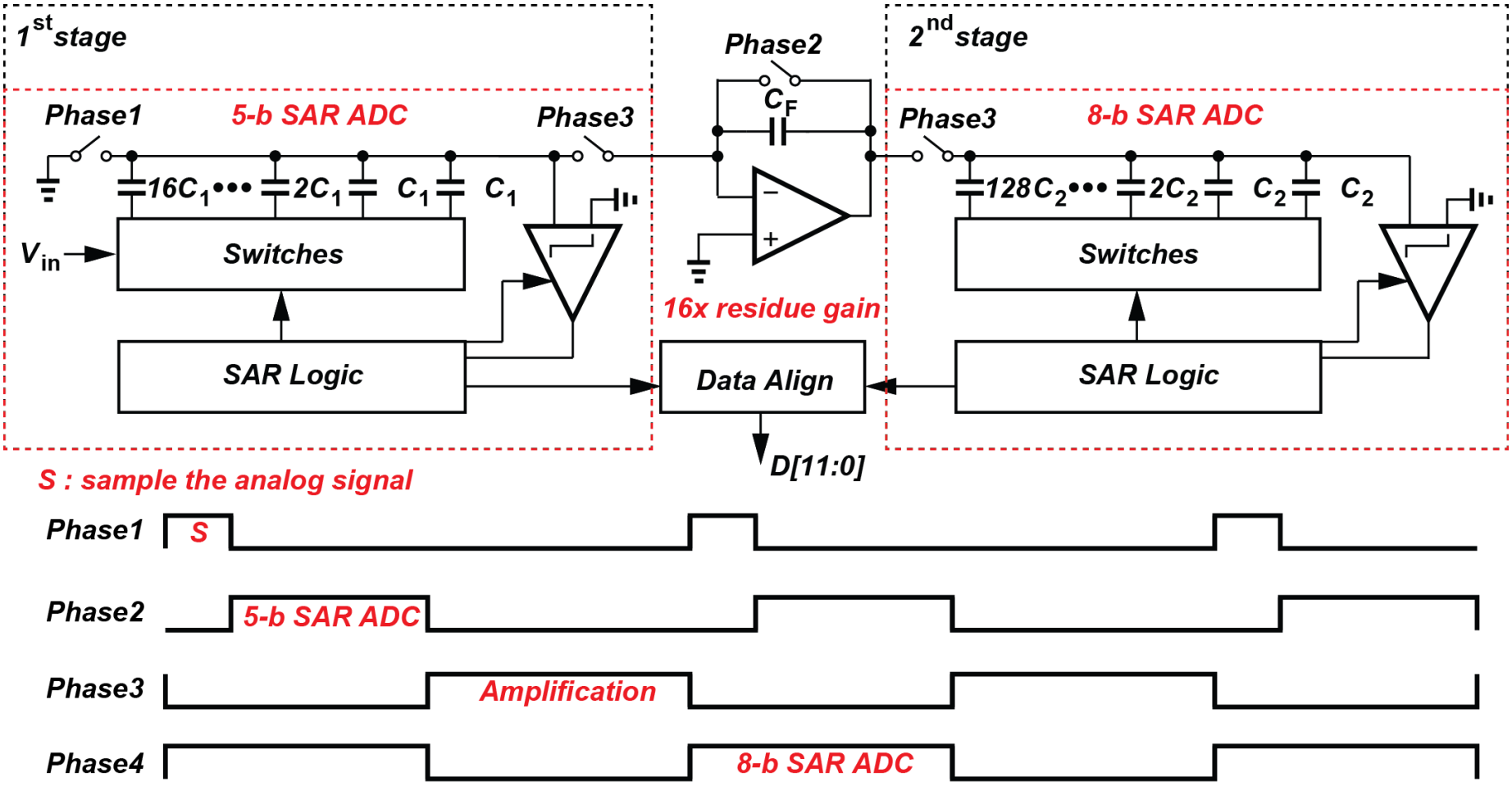
October 7, 2016

Chen-Kai Hsu

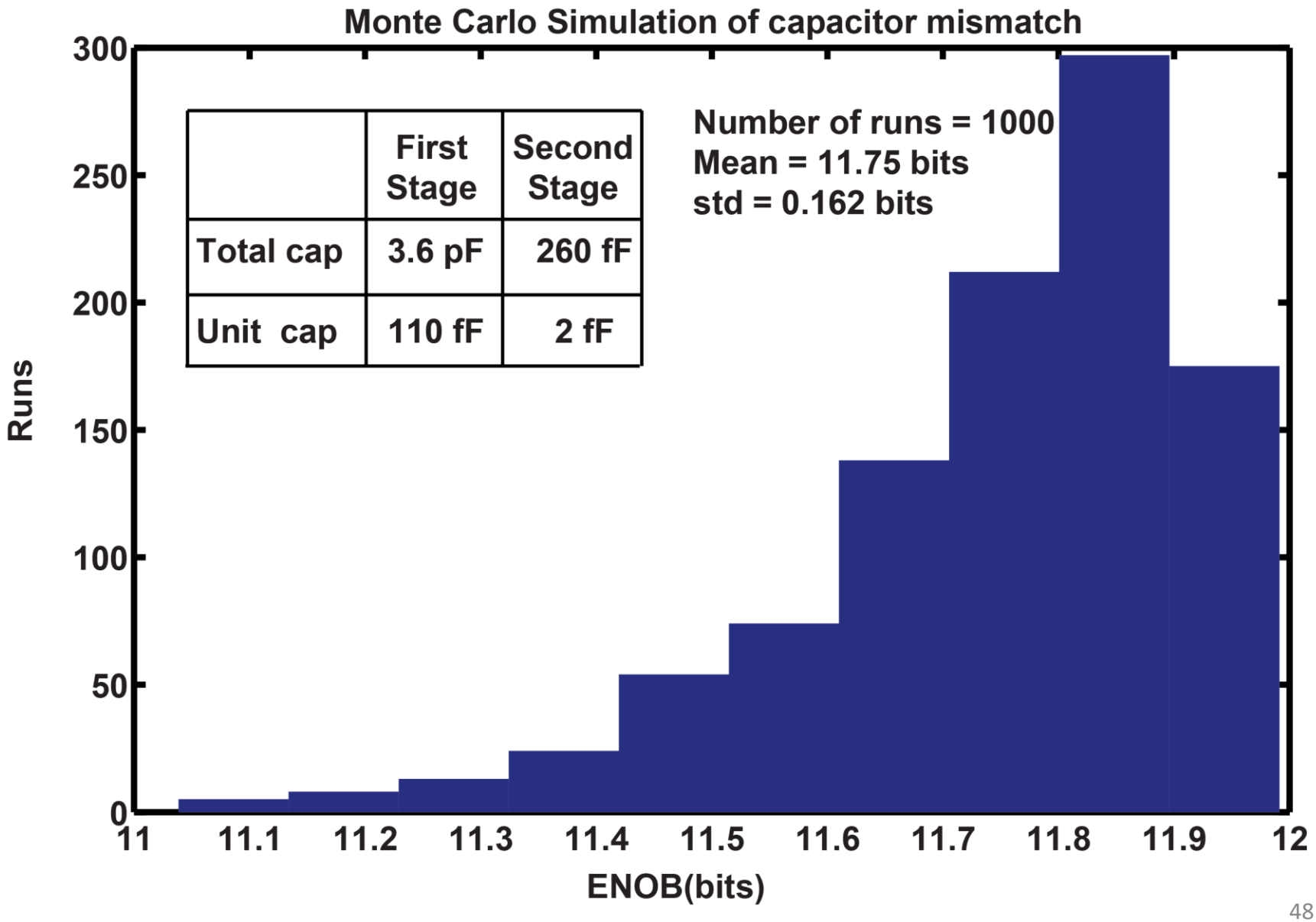
- Education
  - M.S., National Taiwan Univ., 2015
  - B.S., National Chung Cheng Univ., 2012.
- First year PhD student at UT Austin.
- My research interests include high-performance data converters, sensor interface, and mixed-signal circuits
- Process experience:
  - CMOS 0.18um / 90nm / 40nm.
- Some Research experience:
  - Low-power high-speed Pipeline ADC in 90-nm technology.
  - Low-power SAR ADC in a 0.18-um technology for smart badge.
- Publication:
  - **Chen-Kai Hsu** and Tai-Cheng Lee, "A Single-Channel 10-b 400-MS/s 8.7-mW Pipeline ADC in a 90-nm Technology." *IEEE Asian Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 233-236, Xiamen, China, Nov. 2015.

Architectural Level Plan

The ADC is a 5 + 8 bit two-step structure with 1 bit inter stage redundancy to generate a 12-bit output.



Top Level Consideration



Top Level Consideration

- **Open-loop gain consideration:**

By charge conservation, the output of a residue amplifier can be derived as:

$$V_{RES} \approx \frac{32C_1}{C_F}\left(VIN - \frac{1}{32}(16B_1 + 8B_2 + \cdots + B_5)V_{REF}\right)(1 - \text{Error})$$

Where Error = $\frac{32C_1 + C_P + C_F}{AC_F}$

Therefore, in order to provide **16x** close-loop gain, we need a **78dB** open-loop gain amplifier to satisfy 8-b accuracy(1/2LSB).

- **Bandwidth consideration:**

Assuming amplifier is a single pole system, we have:

$$V_{RES} = V_{STEP}(1 - e^{-t/\tau}) \qquad \tau = \frac{1}{\omega_{3dB}}$$

At least, 1.27GHz unit-gain bandwidth is needed.

Top Level Consideration

Assuming 2 stage Miller compensated OTA:

$$Phase\ Margin = 90° - \arctan(\frac{g_{m1}/C_C}{g_{m2}/C_L})\ ;$$

$$g_m = \frac{I_{tail}}{V_{overdrive}}$$

For Phase Margin at least greater than 65 degree,

- $I_{stage2} = I_{stage1}$ ⇨ $C_C=2.2C_L$ (V_{eff} are the same at each stage)
- C_L =260fF(decided by monte carlo simulation). ⇨ C_C=572fF
- g_m=2*pi*1.27GHz*C_C =4.5mS
- So, $I_{stage2} = I_{stage1}$ = 0.45mA (assume $V_{overdrive}$=0.1 V)

Estimated Power

Power estimaton of this work	
Total	> 3.6 mW
Amplifier	> 1.08 mW
Ref. buffer	2 mW
others	0.9 mW

*others include
1.digital circuit
2.bootstrap switch
3.clock buffer

	This work	(1) VLSI 2010
Architecture	Pipeline SAR	Pipeline SAR
Calibration	No	No
Technology	TSMC 65 nm	65 nm
Resolution	12 bits	12 bits
Supply Voltage	1.2 V	1.3 V
Sampling Frequency	40 MHz	50 MHz
ENOB	> 11.2 bits	10.7 bits
Power	> 3.6mW	*3.5mW
Input Range(diff.)	2 Vp-p	2 Vp-p

* Power excluding reference buffer

Specification Review

	Specification	Confidence
Technology	TSMC 65 nm	OK
Supply Voltage	1.2 V	OK
Sampling Frequency	40 MHz	OK
ENOB	11.2 bits	a little tough
Power	< 20 mW	OK
Input Range	2 Vp-p	OK

Schedule

Expected Timeline before tapeout

Oct. ‘16	Nov. ‘16	Dec. ‘16	Jan. ‘17	Feb. ‘17 to Apr. ’17
Amplifier Design	Stage1 Design	Stage2 Design	Whole chip Optimization	Layout and post-simulation

Reference

1. C. C. Lee and M. P. Flynn, “A SAR-assisted two-stage pipeline ADC,” *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 859–869, Apr. 2011.

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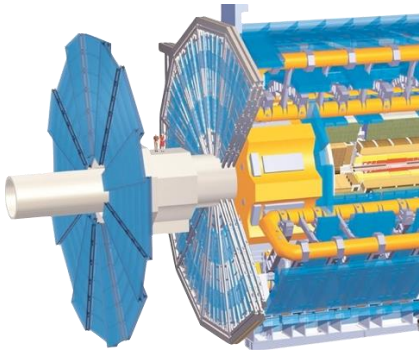
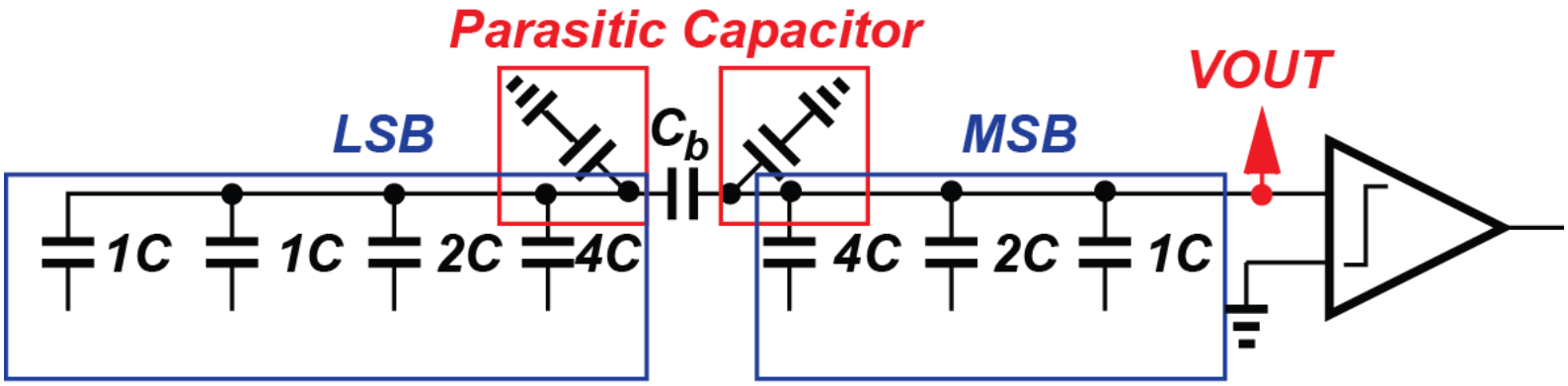
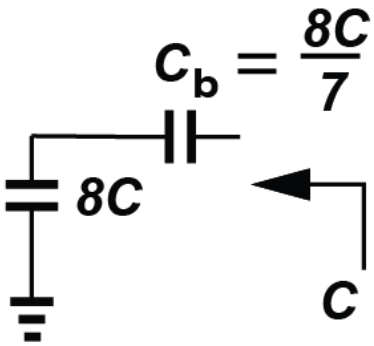


Back up slides

Solution1 for stage2

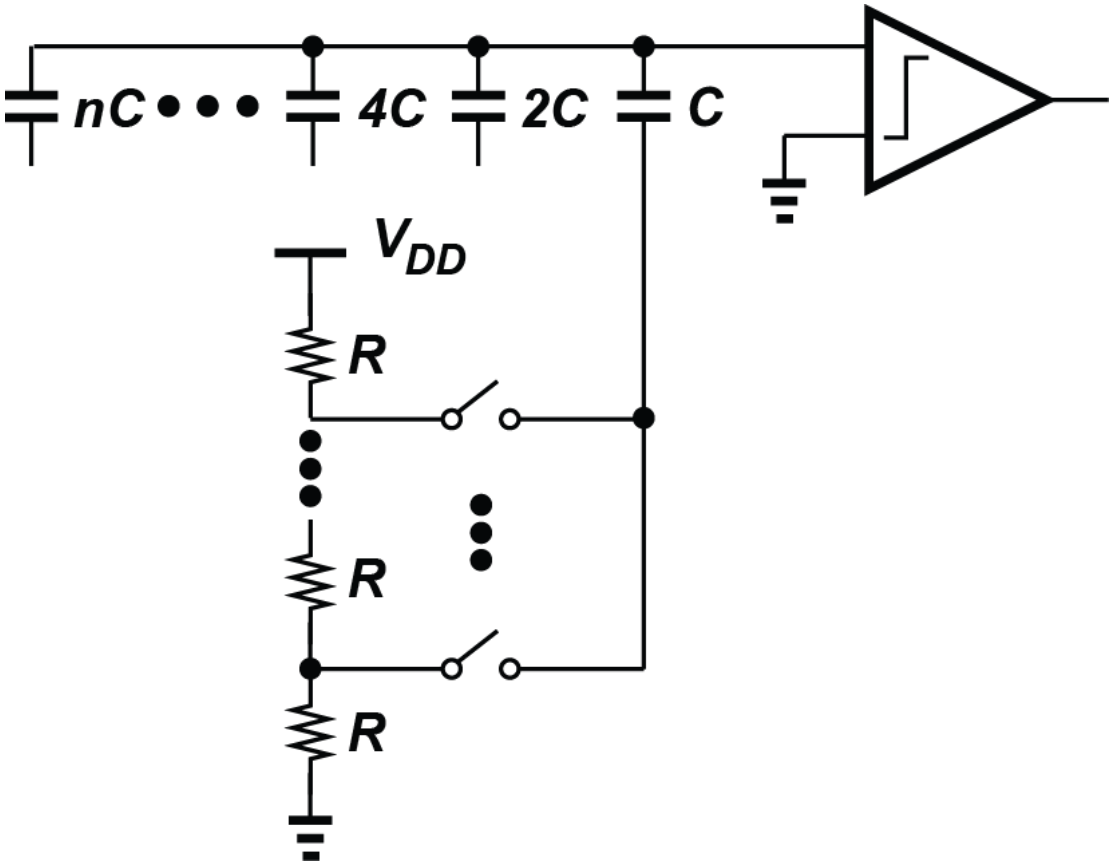
1. Bridge Capacitor Array





Solution2 for stage2

Hybrid DAC



Clock Buffer